NOVEL DIGITAL SYSTEMS DESIGNS FOR SPACE PHYSICS INSTRUMENTATION

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Abstract

This thesis presents the development of two novel Space Plasma Physics instruments.
The few costly space weather missions (SOHO, CHAMP etc.) are justified on the qualitative basis of technological capabilities, such as high-resolution magnetometry, UV, X-ray and stray light imaging power etc. Space weather can also be studied from ground. The demands for ground measurements have increased significantly over the recent years (e.g. THEMIS field-of-view is enhanced by ground instruments). Costs associated with cleanroom procedures, space qualification, launch and operation are avoided. Low-cost ground instrumentations are easier to maintain and upgrade. Controlled high-resolution experiments demand the development of low-noise, interference immune, multi-frequency, multi-bandwidth, multi-dynamic range and multi-integration time instrumentations. Frequency ranges outside the bands of spaceborne instruments are demanded, increasing the range of scientific observations. In-situ data timestamping, real-time clock support and geographical position are demanded for synchronisation with other networked data sets. Performing experiments using different parametric sets or autonomous event-triggered observations demand programmable and dynamically reconfigurable instrumentations.

This thesis initially presents the design of a custom dual-channel cross-correlator data acquisition system. The cross-correlator is later incorporated into the two novel riometer (PRIAMOS) and magnetometer (DIMAGORAS) systems. The primary goal of Priamos is the upper-atmospheric absorption measurement of the highly energetic galactic electrons emissions superimposed on the Cosmic Microwave Background and other last scattering surface galactic and extragalactic radio astronomical background emissions. Priamos surveys accurate right ascension positions with an unprecedented combination of frequency, bandwidth and sensitivity, compared to existing widebeam riometers, providing in-depth observations of the different Space Physics events. It is the first riometer equipped with a programmable saturation protection circuit, enabling measurements of strong Solar Radio Emissions. Dimagoras measures the Earth's field disturbed magnetic flux density due to Space Physics events. The results of a novel applied design methodology for engineering low-power macroscale optimised sensors, also suitable for aerospace applications, are presented, which yielded to the development of a tri-axial fluxgate sensor. Space Physics events are measured in detail due to the receiver's programmable dynamic range, resolution and integration time.

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Abbreviations

ADC: Analogue-to-Digital Converter

AFE: Analogue Front End

AGONET: Antarctic Geospace Observatory NETwork

ALU: Arithmetic Logic Unit

AML: Address Matching Logic

AMR: Anisotropic Magnetoresistance

API: Applications Programmer Interface

ARIES: Advanced Riometer Experiment in Scandinavia

ASIC: Application Specific Integrated Circuit

ATM: Asynchronous Transfer Mode

BB: Baseband

BGS: British Geological Survey

BJT: Bipolar Junction Transistor

BM: Butler Matrix

BPF: Band-Pass Filter

Bps: Bits Per Second

BRAM: Block RAM

BW: Bandwidth

CAD: Computer Aided Design

CCS: Code Composer Studio

CE: Clock Enable

CIC: Cascaded Integrator Comb

CLB: Configurable Logic Block

CMB: Cosmic Microwave Background

CMOS: Complementary Metal-Oxide Semiconductor

CN: Cosmic Noise

CNA: Cosmic Noise Absorption

COSPAR: Committee on Space Research

CPCI: Compact PCI

CPLD: Complex Programmable Logic Device

CPU: Central Processor Unit

CRC: Cycle Redundancy Check

CSMA/CD: Carrier Sense Multiple Access with Collision Detection

DAQ: Data Acquisition

dB: Deci-Bells

DAC: Digital-to-Analogue Converter

DCE: Data Circuit-Terminating Equipment

DCM: Digital Clock Manager

DDC: Digital Down Converter

DDS: Direct Digital Synthesiser

DIGISONDE: Digital Ionosonde

DLL: Dynamic-Link Library

DMA: Direct Memory Access

DMI: Danish Meteorological Institute

DNR: Dynamic Range

DPS: Digisonde Portable Sounder

DR: Dynamic Range or Data Rate

DRC: Design Rule Check

DSK: DSP Starter Kit

DSP: Digital Signal Processor

DTE: Data Terminal Equipment

EEPROM: Electronically Erased Programmable Read Only Memory

EISCAT: European Incoherent Scatter

EMC: Electromagnetic Compatibility

EMF: Electromotive Force

EMIF: External Memory Interface

EVM: Evaluation Module

FCS: Frame Check Sequence

FDTD: Finite Difference Time Domain Method

FIT: Finite Integration Theory Method

FFT: Fast-Fourier Transform

FTP: File Transfer Protocol

FIFO: First-In First-Out

FIR: Finite Impulse Response

FPGA: Field Programmable Gate Array

FSM: Finite State Machine

FWFT: First-Word Fall-Through

GMI: Giant Magnetoimpedance

GPIO: General Purpose Input/Output Port

GPRS: General Packet Radio Services

GPS: Global Positioning System

GSM: Global System for Mobile Communications

HF: High Frequency

HF: Half-Full

HPBW: Half-Power Beam Width

HPI: Host Port Interface

HW: Hardware

I: In-Phase Component of a signal

IAGA: International Association of Geomagnetism and Aeronomy

IC: Integrated Circuit

IF: Intermediate Frequency

IFG: Inter Frame Gap

IMAGE: International Monitor for Auroral Geomagnetic Effects

IMF: Interplanetary Magnetic Field

IMO: INTERMAGNET Magnetic Observatory

INTERMAGNET: International Real-time Magnetic Observatory Network

IONOSONDE: Ionospheric Sounder

IP: Internet Protocol

IRIS: Imaging Riometer for Ionospheric Studies

ICSU: International Council of Scientific Unions

ISA: Instruction Set Architecture

ISM: Interstellar Medium

ISDN: Integrated Services Digital Network

ITU: International Telecommunication Union

JTAG: Joint Test Action Group

LBI: Long-Baseline Interferometry

LC: Logic Cell

LO: Local Oscillator

LPF: Low-Pass Filter

LSB: Least Significant Bit

LUT: Look-Up Table

MAC: Media Access Controller

MAC: Multiply-and-Accumulate

McASP: Multi-Channel Audio Serial Port

McBSP: Multi-Channel Buffered Serial Port

MDS: Minimum Detectable Signal

MEMS : Micro-Electro-Mechanical Systems

MIPS: Mega Instructions Per Second

MMACS: Million MACs per Second

MMIC: Monolithic Microwave Integrated Circuit

MoM : Method of Moments

MPI: Max-Planck Institute

MSB: Most Significant Bit

MSPS: Mega Samples Per Second

MTBF: Mean Time Between Failure

NCD: Native Circuit Description

OIP: Output Intercept Point

OS: Operating System

OSI: Open Systems Interconnection Reference Model

OTR: Out-Of-Range

PAR: Place And Route

PCA: Polar Cap Absorption

PCB: Printed Circuit Board

PCI: Peripheral Components Interconnect

PCI-X: PCI Express

PENGUIn: Polar Experiment Network for Geophysical Upper-Atmosphere Investigations

PMC: PCI Mezzanine Card

PPM: Parts Per Million

PPP: Point-to-Point Protocol

PSD: Phase Sensitive Detector

PSM: Programmable Switching Matrix

Q: Quadrature Component of a signal

QDC: Quiet Day Curve

RADAR: Radio Direction and Ranging

RAM: Random Access Memory

RF: Radio Frequency

RIOMETER: Relative Ionospheric Opacity Meter for Extra - Terrestrial Electromagnetic Radiation

ROM: Read Only Memory

RTC: Real-Time Clock

RTL: Register Transfer Logic or Level

SAMA: South Atlantic Magnetic Anomaly

SAMNET: Sub-Auroral Magnetometer Network

SANAE: South African National Antarctic Expedition

SCAR: Scientific Committee for Antarctic Research

SCNA: Sudden Cosmic Noise Absorption

SCOSTEP: Committee On Solar-Terrestrial Physics

SFD: Start Frame Delimiter

SFDR: Spurious Free Dynamic Range

SID: Sudden Ionospheric Disturbance

SIM: Subscriber Identity Module

SNR: Signal – to – Noise Ratio

SoC: System-on-Chip

SPEARS: Space Plasma Environment and Radio Science

SRE: Solar Radio Emission

SQUID: Superconducting Quantum Interference Device

TCP: Transmission Control Protocol

TI: Texas Instruments

UART: Universal Asynchronous Receiver and Transmitter

UCF: User Constraint File

UPS: Uninterrupted Power Supply

USP: Unit of Space Physics

UTOPIA: Universal Test and Operations PHY Interface for ATM

UV: Ultraviolet

VHDL: Very High Speed Integrated Circuits Hardware Description Language

V/I: Voltage-to-Current converter

VLA: Very Large Array

VLBA: Very Long Baseline Array

VLIW: Very Long Instruction Word

WMM: World Magnetic Model

X-Bus: Expansion Bus

XDS: Extended Development System

ZBT: Zero Bus Turnaround

Chapter 1.
Introduction

The aim of the thesis is to design two novel scientific instruments for measurements of complex space physics events, namely a riometer (Relative Ionospheric Opacity Meter for Extra Terrestrial Electromagnetic Radiation) and magnetometer. The instruments have been given the acronyms Priamos (Programmable Riometer for in-depth Ionospheric and Magnetospheric Observations) and Dimagoras (Digital Magnetometer for Oracular upper-Atmospheric Studies). The novelties of the two systems are achieved by formulating and applying design methodologies resourced from the research fields of Space Physics Instrumentation, hardware, electronics, sensor systems, digital signal processing and Radio Astronomy.

A riometer measures the cosmic microwave background (CMB) absorption by the upper-atmospheric layers. Statistical analysis of the captured data yields to identification of space physics events. A riometer is categorised into passive Radio Astronomy instrumentation, since no transmitters are used. A magnetometer measures the strength of magnetic fields. Within the thesis, a magnetometer or a sensor measure the Earth's magnetic field variation. The main contribution due to the Earth's core and crustal fields is removed. The system measures the aggregate disturbed magnetic flux density due to space physics events. Both instruments provide an indirect method for studying space weather conditions.

Chapter 2 retrieves information from the six pre-mentioned research fields, with relevance to the two systems. The CMB, radio stars emissions, space physics events and noise induced from the receiver itself is the input to the riometer. Due to the low-frequency of operation, macroscale antennas are being used suitable for Radio Astronomy observations. A comparison between riometers and radio telescopes clarifies the main differences between the two classes of Radio Astronomy instruments. Existing widebeam and imaging riometer instrumentations and specifications are presented with emphasis on their scientific significance.

The Earth's core magnetic field, Earth's crustal fields and the aggregate disturbed magnetic flux density due to space physics events and any induced continental or sea fields is the input to the magnetometer. A systematic comparison between the available sensors and resulting analogue and digital magnetometers is presented. Reviewing ground-based and spaceborne magnetometers set the target specifications for the new system.

The research, so far, assisted in identifying key system parameters, setting an initial set of specifications and appreciating the scientific importance of the two systems in indirectly measuring space weather conditions. For instance, in widebeam riometer observations, the temporal resolution is inversely proportional to the bandwidth. The integration time may be reduced when the bandwidth is increased. The receiver's parameters are also affected by these variations, such as the noise figure which is proportional to the bandwidth.

It was soon realised that two digital systems architectures are required to fulfil the specifications and, to provide the expected processing power and programming flexibility. The research was directed into the available digital systems design methodologies. A comparison between the available hardware technologies is presented.

Field programmable gate arrays (FPGAs) or digital signal processors (DSPs) are commonly used for fast prototyping of algorithms and hardware designs. However, FPGAs have overcome DSPs over the recent years in terms of processing power, logic capacity, popularity amongst hardware designers and the ever increasing FPGA applications.

Recent developments in radars, remote sensing instruments, radar interferometers, sounding rockets, standard, nano- and pico- satellites and spacecrafts, robots for space exploration etc. are based on reconfigurable FPGA solutions. Specifications require future Deep Space communications developments to implement multi-protocol and reconfigurable system-on-chip (SoC) transceiving systems. Priamos and Dimagoras are implemented using reconfigurable FPGAs.

Chapter 3 evaluates the performance of the cross-correlation algorithm between non-identical signals. The correlator is the major DSP function in every radio interferometer. Antenna-array theory is applied to derive the cross-correlation and auto-correlation functions to be modelled in hardware. A dual-channel cross-correlator system is developed and data acquisition is achieved via the 32-bits/33 MHz PCI bus. The correlator is seriatim being reused by both Priamos and Dimagoras systems.

Chapter 4 describes the feasibility study, RF Receiver Unit and peripheral hardware design for Priamos. Priamos has been through many design iterations before finalising the specifications, hardware design, computer architecture and instrumentation. The final version provides a set of novel specifications and significantly improved performance over existing widebeam riometers. The RF receiver design study indicates that removing the extensively used noise balancing technique and continuously processing the input signal provides an improvement of 3 dB. The direct sampling architecture provides an improvement of 6 dB over multi-stage receivers.

The receiver tunes to CMB emissions in the frequency range of 1 – 60 MHz. The programmable bandwidth of observation is in the range of 3 KHz – 1 MHz. The receiver has a programmable dynamic range up to 175 dB, so that saturation is avoided during strong solar radio emissions of type III and IV. The RF Receiver Unit can be installed close to the antenna for 0 dB transmission line losses. A programmable master oscillator interface generates accurate frequency sampling signals up to 250 MHz. A programmable GPS interface and instrumentation is presented for in-situ data timestamping.

Chapter 5 proceeds to the hardware design of the Priamos DSP Engine Unit. The implementation of a digital band-pass filter operating at the sampling frequency is considered first. The excessive DSP power requirements indicated that a digital down conversion stage is required before the FPGA. The DSP Engine Unit has been through three design iterations before the optimum configuration is selected and developed.

The first iteration requires a high-performance DSP evaluation kit to be interfaced by seven other prototype boards, including the RF Receiver Unit. Control over the system is limited, many programmable features are disabled and a co-processor on a

peripheral bus is still required to fully control the system. A custom DSP-based with FPGA co-processor system is considered next. The resulting hardware complexity and prototyping cost yielded to an FPGA-based solution, which is evaluated and the design is presented.

The FPGA-based Priamos DSP Engine Unit supports over 300 commands for real-time programming and reconfiguration of the system. The computer architecture is based on eight mega-functions that programme or reconfigure the FPGA, RF Receiver Unit, GPS receiver, external memory, master oscillator and glueless UART, USB 2.0 or 10/100 Mbps fast Ethernet interfaces. Priamos is the first multi-port riometer.

The system features programmable functions such as, dual-down conversion processing, auto-correlation, variable sampling frequency, universal time clock, in-situ data timestamping, storage up to 144 hours or real-time transfers. The DSP Engine Unit is independent of the antenna type being used, consisting a prototyping platform for other space physics instrumentation projects.

Chapter 6 describes the feasibility study and system analysis for Dimagoras. The analysis of existing and planned magnetometers indicated that magnetometer design is evolving rapidly. There are two general design methodologies. The first methodology involves designs where a new sensor is developed and the receiver's electronics are adjusted accordingly. The second category covers designs using an existing sensor and the receiver's architecture is adapted. The reviewed systems lack the flexibility in terms of signal processing and are tied to one sensor, operating frequency, bandwidth and dynamic range. Variable integration time instrumentations exist.

For Earth's field measurements the extra flexibility can be omitted. The study of space physics events requires flexibility in hardware and software processing. For instance, programming and expanding the dynamic range by digitally controlling the analogue circuits allows space physics events to be captured at the full-scale edges of the hardwired dynamic range that would otherwise be missed.

A novel applied design methodology for engineering low-power macroscale optimised fluxgate sensors for measurements of space physics events is presented. The basic sensor saturates for an excitation current of +/- 250 mA. The optimised sensor saturates at +/- 60 mA. Power consumption is reduced by a factor of 16 and over 32 for existing spaceborne instrumentations. The low noise factor qualifies the macroscale optimised sensor for spaceborne applications. Clean room procedures and material handling are essential for maintaining both the supermalloy's and magnetic shield's high-permeability values. The sensor's sensitivity of 151 uV/nT amply covers the Earth's magnetic field variation. A tri-axial sensor is built by appropriately assembling three single-axis sensors. The sensor stipulates the DSP requirements.

Chapter 7 proceeds to the hardware design of the remaining Dimagoras system, built on the experience obtained from Priamos. The Priamos DSP Engine Unit can also be reused by modifying the FPGA's VHDL code. Dimagoras implements a novel multi-frequency and multi-bandwidth scheme supporting any fluxgate sensor tuned in the frequency range of 1 KHz up to 1.5 MHz. Most of the sensors are tuned up to 100 KHz. However, oversampling increases the system's resolution and determines the noise performance and optimum frequency of operation. Dimagoras is one of the few multi-port magnetometers.

Finally, conclusions are drawn to summarise the research work and to highlight the major engineering achievements presented throughout the thesis. Future work is essential for Dimagoras in two aspects.

Other materials and sensor designs can be macroscale implemented. For instance, a new material was recently found with better specifications than supermalloy. It can be used to reduce power consumption even further using the same dimensions of the prototype cores. The optimisation technique is directly applicable in the microscale. Since nanowires exist, it is worthwhile investigating if nanotechnologies support it as well. A radiation hardened MS ASIC or FPGA solution can be devised that could qualify for Space.

Scientific software development can be expanded to include the contribution of space physics magnetometers into the World Magnetic Model for space weather short term predictions. The World Magnetic Model takes into consideration the altitude variation, so the predictive model is applicable to airborne magnetic sensors applications.

The following chapter provides information on the scientific significance of riometer and magnetometer instrumentations, as well as, digital systems design methodologies that inspired and challenged the hardware design of Priamos and Dimagoras.

Chapter 2.
Background Theory

2.1 Background

A riometer is a passive radio astronomy instrument measuring the radiation intensity received from different parts of the sky and the corresponding Cosmic Noise (CN) Absorption (CNA) by the lower ionospheric layers [1].

The CMB is the major source of the sky brightness at centimetre wavelengths [2]. This corresponds to a temperature of 2.73 K and it is used to derive the brightness intensity of many other wavelengths in the near region. However, riometers operate at long radio wavelengths and up to 50 MHz. At these frequencies the brightness of the sky is more intense than expected from the CMB by itself. At 35 MHz the effective temperature is over 100,000 K.

This radiation is due to highly energetic galactic electrons radiating at these frequencies. Their spectrum is different to the black body's spectrum, safely assumed for the calculation of the different near-centimetre wavelengths cases, since the derivations do not include any radiation processes. This is because radiation used to equipoise matter at an early cosmic evolution stage, and maintained its spectrum in any seriatim expansion and cooling stages [3].

Superimposed on CN is any induced noise from the receiver itself. Including the emissions from the different radio stars at the tuned frequency, the riometer is presented with very low-power levels to be measured. Some of these radio sources have angular sizes of only one arcsec and can only be measured by radio telescopes at higher frequencies. Imaging riometers use widebeam antennas to deliberately exhibit resolution in the range of 40,000 arcsec/beam covering wider sky areas. The strongest of these sources could be detected by riometers, if more directional antenna phased-array systems are built with higher spatial resolution for resolving the acquired power measurements. Introducing higher power gain systems is not an option for the passive riometers. This applies to radio telescopes in active mode.

Radio telescopes are better operated in the frequency range 1.4 – 15 GHz, where CN radiation, atmospheric absorption in general, and ionospheric or tropospheric phase instabilities are kept to a minimum. The technology employed and the research extracted from the deployment of radio telescopes had a strong impact in the development of modern sciences.

Since 1963, Arecibo in Puerto Rico (50 MHz-10 GHz) is the world's largest single-dish (305 m diameter, 50m depth) radio telescope with a 2.5 MW (BWmax = 2 MHz) planetary radar transmitter. After a short transmission (2 us - 2.1 ms), the target's size and distance is analysed by the returning echoes [4]. Long-baseline interferometry (LBI) increased resolution to x100,000 from the observer. Since 1980, the LBI Very Large Array (VLA) near Socorro, New Mexico (74 MHz-50 GHz, 0.04 arcsec maximum resolution at 43 GHz, 24 arcsec at 74 MHz) is the world's largest array of 27 25 m-diameter Y-shaped radio telescopes [5]. Since 1993, the Very Long Baseline Array (VLBA) controlled by the Array Operations Centre in Socorro, New Mexico (0.0002 arcsec maximum resolution at 43 GHz) is the world's largest astronomical instrument of ten 25 m-diameter radio telescopes [6].

In phased-array riometer systems two strong radio sources are additionally superimposed on background noise. Due to the diurnal Earth's rotation first the extragalactic source Cygnus A and, then, the supernova remnant Cassiopeia A pass through the antenna-array field-of-view. Cygnus A radio galaxy, discovered by Hey in 1946 [7], is in fact one of the strongest radio sky sources. The youngest supernova remnant in the Galaxy (300 years old) Cassiopeia A is the brightest radio source in the sky [8], but its radio emission is progressively decreasing.

CN is absorbed or attenuated as it passes through the Earth's atmosphere at certain frequencies, due to the complex solar wind–magnetospheric–ionospheric system. Highly-energetic particles with energies between 10 KeV and 100 KeV precipitate through the upper atmosphere, increasing the fractional ionospheric ionisation, especially at altitudes where electron motion is collision-dominated [9]. Absorption is a partial release of the CN energy to heat through electron collisions and is proportional to both the energy flux and observation frequency.

The influence of space weather conditions over the Earth's magnetic field can be measured by magnetometers. A basic magnetometer measures magnetic fields (e.g. a fluxgate magnetometer measures the Earth's magnetic field) or magnetic moment (e.g. a vibrating or gyratory magnetometer). The name magnetic sensor signifies sensors working on magnetic principles and in this thesis, sensors that measure the Earth's magnetic field.

Currently, the research conducted on sensors is based on miniaturisation by using new materials. Non-semiconductor sensors, such as fluxgates, induction sensors etc. are already using micro-technologies. Micro-coils and micro-relays using modern micromachining processes are described in [10]. The application of amorphous materials such as wires and tapes to sensors in general is analysed in [11].

Depending on the nature of the magnetic field under measurement, different ranges exist within the universe. Within the Space Physics context, magnetic fields of interest are the galactic magnetic field ($B \approx 0.2$ nT), Earth's magnetic field ($B \approx 60$ uT), white dwarf's ($B \approx 1$ kT) and pulsar's ($B \approx 100$ MT) [3].

A research field of interest is how the Earth's magnetic field was created, which effectively answers the question on how polarised/centralised magnetic fields can be created on other planets (e.g. Mars) to recreate Earth-like atmosphere and living conditions. Acuna [12], principal investigator of the magnetometer/electron reflectometer instrument on-board NASA's Mars Global Surveyor orbiter, verified that stronger than expected magnetic field of planetary origin exists on Mars.

Mars has no centralised field of internal origin, but must have had one in the past, when the crust acquired intense magnetisation, probably by cooling in the presence of a similar to Earth magnetic field (thermoremanent magnetisation). Planets like Jupiter, Saturn, Uranus, Neptune and Earth generate their magnetic fields by means of a dynamo made up of moving molten metal at the core. This metal is a good conductor of electricity and the rotation of the planet creates electrical currents deep within the planet that give rise to the magnetic field.

Another question that puzzled the author is what would happen in case the poles are reversed. It is well known that the Earth's magnetic field is gradually weakening ($\approx$ 0.1% per year), that is why the research on low frequency gravity waves, and there is a possibility in the near future of pole reversal. Of course, this requires an internal (high unlikely) or external strong threshold (e.g. a strong gravity source passing close to Earth). There are many different points of view, all supported mainly by Russian and US scientists. One recent theory about pole reversal is in [13].

The thesis is concerned with the novel hardware design of two riometer and magnetometer systems, therefore, the following sections are related to the different types of riometers and magnetometers and long-term scientific observations. The chapter concludes with the different hardware design techniques that can be used to implement the two systems.

2.2 Riometry

The concept of riometry was introduced over 50 years ago [14] to collect information about the state of the lower ionosphere and to investigate phenomena, such as auroral disturbances. Thereafter, many applications and scientific literature have been derived. It is a passive radio wave experiment, since no transmitters are used. A riometer has also been used for studying the atmosphere of Mars [15].

Riometers consist of low noise, sensitive receivers equipped with calibration circuits. Amplitude and, in some systems, phase, can be measured of the received sky radiation. A single vertical antenna with the main lobe in the direction of local zenith can be used to form a widebeam riometer. CNA varies according to the Earth rotation, but remains constant for a repeated Local Sidereal Time. In contrast to widebeam riometers, only imaging riometers attracted detailed attention in recent years from the scientific community and funding bodies.

2.2.1 Widebeam Riometers

Widebeam riometers have a single antenna above a ground plane and have been reported to operate at frequencies of 16.6 [12], 20, 20.5, 21.3 [17], 25 [17], 27.6, 29.7, 29.9, 30, 32, 32.4, 35, 38.2 and 51.4 MHz and bandwidths of 15 to 250 KHz. At frequencies below 20 MHz the cosmic radio waves are often obliterated even before reaching the ionosphere. Over 50 MHz, absorption is virtually undifferentiable from the CMB [18].

Known widebeam riometers located in the northern and southern hemispheres are red marked in Fig. 2.1 and 2.2, respectively. The antenna is usually a broadbeam design of a vertical three element Yagi, two parallel horizontal dipoles or a circularly polarised cross-dipole with a beamwidth in the region of 60°. Circularly polarised cross-dipole antennas receive both vertically and horizontally polarised transmitted radio signals. They are insensitive to plane polarisation variation due to the ionospheric Faraday rotation effect and for this reason are also used in L-band satellite systems [19].

In riometry, CN is the measurable “signal”. CN has extreme random amplitude, phase and polarisation. If statistically processed, approximates Gaussian random noise. CN is subjected to both interstellar medium (ISM) and ionospheric Faraday rotation [20]. Different emissions in low frequency radio astronomy are due to the synchrotron mechanism, such as Cygnus A, quasar 3C48 etc., and linearly polarised emissions are produced [21]. OH masers from galactic star forming regions form circularly polarised microwave emissions and other interstellar maser sources often are partially linearly polarised [3]. The sources polarisation is randomised due to the magnetic fields direction variations, even within the sources, and by de-facto Faraday rotation. Circularly polarised cross-dipole antennas increase the CN power levels captured, since the random birefringence recombination at the antenna contains both partially linear (horizontal and vertical) and circular polarisations.

Figure 2.1 Northern Hemisphere Widebeam and Imaging Riometers.

Riometer networks have been used for co-ordinated experiments, e.g. auroral substorm measurements [22]. Widebeam riometer networks have measured the moving absorption [23]. The Unit of Space Physics (USP) of the North-West University in South Africa operates two La Jolla [24] parallel-dipole riometers, at 30 and 51.4 MHz in the well-resourced South African National Antrarctic Expedition (SANAE) IV base, commissioned in 1997 [25]. USP operated 3 riometers, at 20, 30 and 51.4 MHz in the SANAE III base, decommissioned at the end of 1994.

The Space and Upper Atmospheric Physics Group of the University of Maryland, US, operates five wideband riometers in Antarctica and one in Alaska, tuned to 20.5, 30, 38.2, 51.4 MHz. The integration time is 1 s. La Jolla riometers are used with two horizontal parallel-dipole antennas [26]. The Danish Meteorological Institute (DMI) operates the Greenland Riometer Array consisting of eleven widebeam riometers [27]. DMI operated a riometer in Andoya, Norway until 2002.

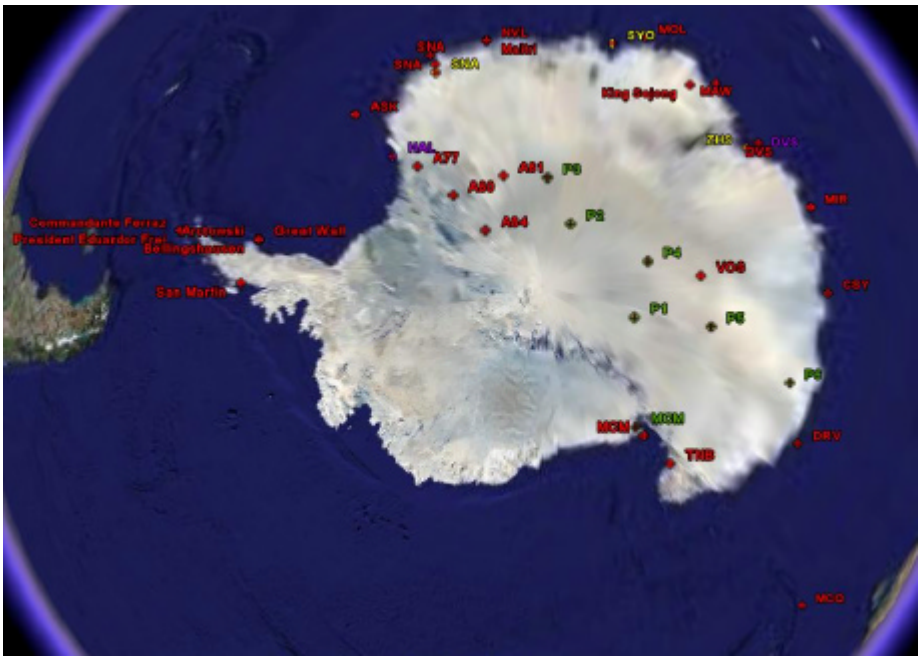


Figure 2.2 Southern Hemisphere Widebeam and Imaging Riometers.

The Physics of Upper Atmosphere and Environment group of the National Institute of Geophysics and Volcanology in Rome, Italy has operated two 30 and 38.2 MHz riometers in Terra Nova Bay, in the Antarctic since 1993. The integration time is 1 s. La Jolla riometers are used with two horizontal parallel-dipole antennas [28].

The Australian Antarctic Division maintains in Antarctica parallel-dipole antenna La Jolla riometers at 30 MHz with a 10 s integration time. The Swedish Institute of Space Physics in Kiruna maintains three La Jolla riometers at 30 and 38.2 MHz. ESRANGE in Sweden maintains a riometer with two beamwidths at 27.6 and 35 MHz. The NORSTAR riometer array of the Institute of Space Research at the University of Calgary consists of an array of fourteen La Jolla riometers at 30 MHz, 5 s integration time, parallel-dipole antenna and bandwidth of 150 KHz [29].

2.2.2 Imaging Riometers

CNA events can be studied in a finer scale by implementing antenna phased-array imaging riometers. The antenna array elements are usually combined by a Butler Matrix [30] to form a set of regularly spaced narrow beams. CN from radio stars and galaxies is constant for a repeated Local Sidereal Time and the source power level depends on the array-beam pointing direction. Imaging riometers measure simultaneously the time-varying CNA intensities in as many directions as possible. Similar to radar and sonar measurement techniques [31], images are derived. In riometry, the images represent instantaneous absorption distributions.

Imaging riometers typically operate at 1 s time resolution and cover a sky area in the region of 250 x 250 km at ionospheric altitude of 90 km. Riometer data can be combined with data from other ground based instruments such as radars [32], magnetometers [33], ionospheric sounders (ionosondes) [34] or digisonde (digital ionosonde) portable sounder (DPS) [35] etc. or satellite remote sensing instruments [36] to study the different disturbance processes in the upper atmosphere. These processes are associated to the energetic particle precipitation during solar flares and geomagnetic storms. These are custom practices for studying space weather.

Basic imaging riometers consist of 16 antennas arranged in 4 x 4 square configurations. 16-beam riometers are green marked in Fig. 2.1 and 2.2. Most of them are located in Antarctic. The University of Maryland, USA provided six imaging riometers for ionospheric studies (IRIS) at 38.2 MHz for each Polar Experiment Network for Geophysical Upper-Atmosphere Investigations (PENGUIn) Antarctic Geospace Observatory NETwork (AGONET). AGONET is conducted by the Scientific Committee for Antarctic Research (SCAR) and a body of the International Council of Scientific Unions (ICSU) similar to the Scientific Committee On Solar-Terrestrial Physics (SCOSTEP) since 1966 and the Committee on Space Research (COSPAR) since 1958. Each PENGUIn (n = 1 - 6) has two riometers for faster data logging, 12-bit sampling resolution and produces a complete radio image every 6 s. The Max-Planck Institute (MPI) for Aeronomy, Germany used to operate a 16-beam IRIS in Ramfjordmoen, Norway until 1995.

The South Atlantic Magnetic Anomaly (SAMA) is characterised by an Earth's minimum magnetic field intensity [37]. To study SAMA, the Southern Space Research Center (INPE) at the southern space observatory (SSO) in Brazil, in collaboration with Nagoya, Takushoku and Kyushu Univesities in Japan installed a 4 x 4 beam IRIS (INPE-SSO) with 1 s time resolution and a 250 KHz bandwidth [38]. The experiment lasted until 1999.

The University of Maryland, USA installed the first IRIS system at the South Pole (SPA) (90° S, 0° E) in 1988 [39]. The system uses 64 cross-dipoles tuned to 38.2 MHz. Butler matrices form 64 in total or 49 effective beams. 64- and 49-beam riometers are yellow and purple marked in Fig. 2.1 and 2.2, respectively. The spatial resolution is about 20 km at 90 km height.

The 49 beams exiting the butler matrices connect to seven riometer receivers. Using time-division switching each riometer is fed with one of the 7 columns of 7 beams. The time resolution is 1 s. Switching is accomplished by dividing each second into 8 time slots. Each one of the 7 beams is monitored for 125 ms. The widebeam output is in the eighth slot. Each output is digitised using 8-bits in the old IRIS design, or 12-bits resolution in the newer version. Data acquisition (DAQ) software stores data for scientific analysis.

The Space Plasma Environment and Radio Science (SPEARS) Group of Lancaster University, has been operating IRIS at Kilpisjarvi (KIL), Finland since 1994 [40-41]. The antenna array consists of 64 antennas. 49 narrow effective beams are produced of angular resolution of 12° half-power beamwidth. Other IRIS systems are installed at DVS, HAL, STF, IQA, LYR, NAL, ZHS, SNA, TJO, SYO, HUS and DMH stations, operating at 30 or 38.2 MHz.

The world's largest field-array IRIS system is operated in the Poker Flat (PKR) Research Range in Alaska. A 256 beam cross-dipole antenna array arranged in 16 x 16 square is used to form 208 effective power beams within the 70° zenith angle [42-43]. The time resolution is 1 s. The viewing area is 400 x 400 km^2 at 90 km. The spatial resolution is approximately 11 km around zenith.

2.2.3 Solar Wind-Magnetospheric-Ionospheric Riometer Events

DAQ results are statistically processed to produce experimental quiet day curves (QDCs). Theoretical QDCs can be produced if a radio sky map is available at the frequency of interest. Knowledge of the antenna's radiation pattern and the system's geographical (or Global Positioning System (GPS)) location are also required. The Lancaster University Riosim Simulator can be used for calculating theoretical QDCs. CNA is the difference between the theoretical and experimental QDCs. CNA is visualised by images and keograms in different coordinate systems. Polar cap absorption (PCA), sudden ionospheric disturbances (SIDs), auroral absorption, solar radio emissions (SREs), scintillation and lightning leave their signature on QDCs. The QDC shows the CN level on a day without absorption, SREs, PCA, SIDs etc.

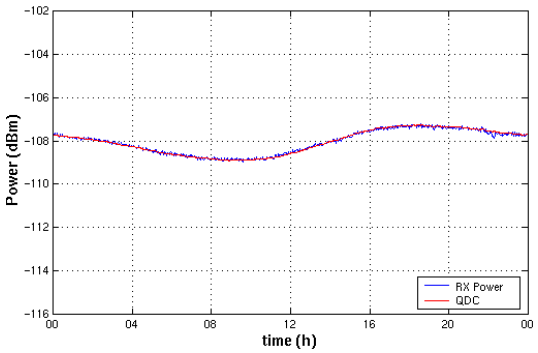


Figure 2.3 Experimental and Theoretical QDCs.

Lancaster University has developed the IRIS data processing Tool kit arranging the data into 14 sidereal days [44]. 590 seconds medians are calculated over each day, resulting in 146 values. The mean of the second and third highest value for each time interval is then calculated, and this is an efficient estimate of the QDC. This is based on the assumption that during this period no disturbances occur. Interpolation is then performed between these values to give one second value over the sidereal day. Other methods for calculating QDCs are in [18] and [45]. IRIS (KIL) widebeam data created the QDCs plotted in Fig. 2.3 for a quiet day.

Sky maps at 22, 30, 38 and 45 MHz are in [46-49], respectively. The digital sky map at 38.2 MHz is in Fig. 2.4. Power is calculated by integrating over the observation hemisphere. The power from radio stars is added. CNA and other events are ignored.

$T_B(\theta,\varphi)$ is the sky temperature and $G(\theta,\varphi)$ the antenna radiation pattern in the direction (θ,φ) in spherical coordinates, as explained in App. B.1. These calculations assume no mismatch losses and a lossless transmission line between antenna and receiver. The received noise power is given by eq. (2-1):

$$P_r = kT_A\Delta f, \qquad (2\text{-}1)$$

Where : $$T_A = \frac{\int T_B(\theta,\varphi)G(\theta,\varphi)\sin\theta d\theta d\varphi}{\int G(\theta,\varphi)\sin\theta d\theta d\varphi} \qquad (2\text{-}2)$$

k is the Boltzmann's constant ($1.38X10^{-23}$J/^{o}K), T_A is the antenna temperature in ^{o}K and ΔF is the bandwidth.

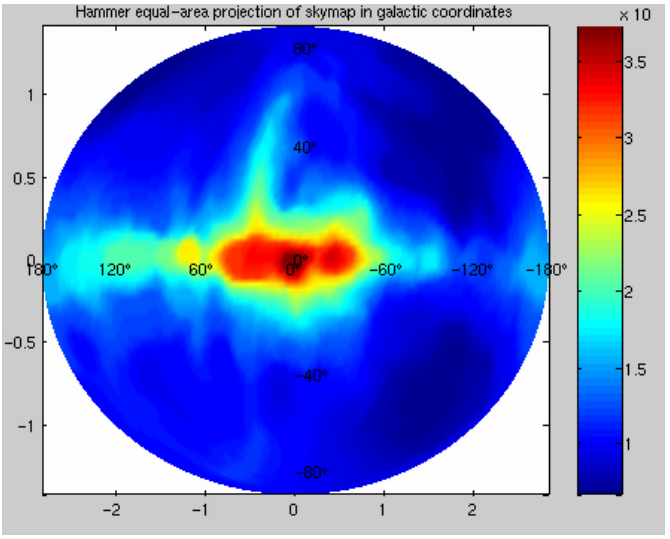


Figure 2.4 Digital Sky Map at 38.2 MHz.

QDCs take advantage of the earth's rotation within a sidereal day and the right ascension values are important. Declination is constant. The right ascension scanning of the galactic plane at 38.2 MHz is in Fig. 2.5. The digital sky map is in galactic coordinates and needs to be converted to celestial coordinates [3]. Celestial coordinates refer to zenith and azimuth values. The cross-dipole's field-of-view over KIL is visualised by projecting the -3 dB points of the radiation pattern on the ionosphere at 90 km altitude as in Fig. 2.6. Similar results can be produced for any antenna type, knowing the current GPS location.

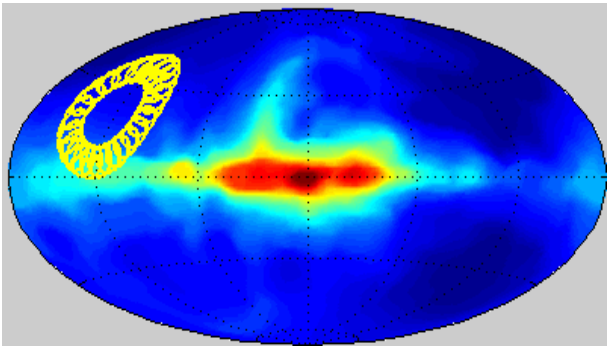


Figure 2.5 Right Ascension Scanning of the Galactic Plane at 38.2 MHz.

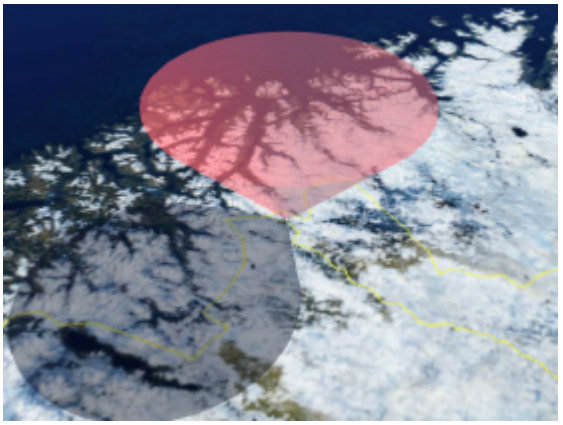


Figure 2.6 Cross-Dipole's Field of View at 90 Km over KIL.

2.2.3.1 Cosmic Noise Absorption (CNA)

CNA [27, 50], in Fig. 2.7, is the ratio of the initial power to the final power in dB, as shown by eq. (2-3). Power is proportional to the square of the measured amplitude.

$$A = 10\log\left(\frac{\text{Pinitial}}{\text{Pfinal}}\right) \qquad (2\text{-}3)$$

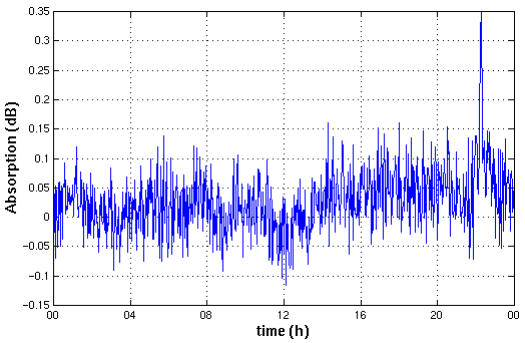


Figure 2.7 Ionospheric Absorption.

2.2.3.2 Auroral Absorption

Aurora has been studied for a long time [51-58]. Absorption values over 10 dB is unusual. Absorption has periodicities from minutes to hours. It is more likely to observe auroral absorption around noon and midnight. Ionosondes are said to "black out" when auroral absorption occurs. Riometer resolution is better than an ionosonde's [59]. Relevant QDCs are in Fig. 2.8, while absorption in Fig. 2.9.

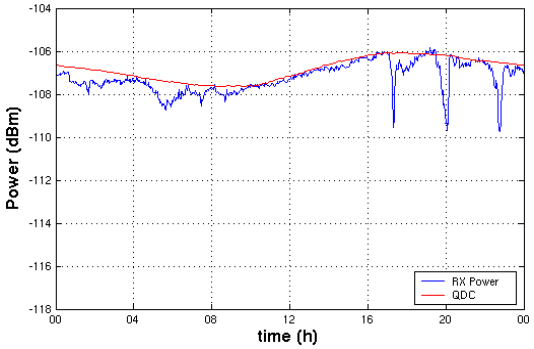


Figure 2.8 QDCs of Auroral Absorption.

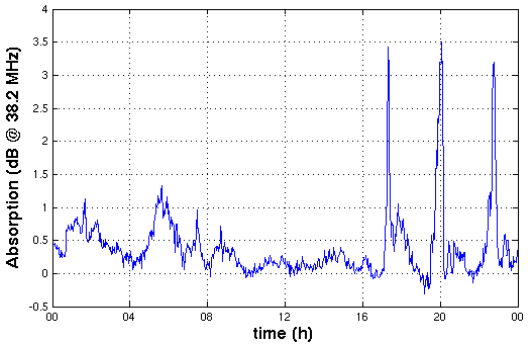


Figure 2.9 Auroral Absorption.

2.2.3.3 Polar Cap Absorption (PCA)

PCA was discovered in 1956 [9]. PCA events occur at high magnetic latitudes covering the whole polar cap. Aurora occurs in certain regions of the polar cap only. PCA is due to high velocity (4.4 x 10^4 Km/s), energetic solar protons (10 MeV) or solar proton events. Protons penetrate the magnetosphere at the polar cap. PCA events can black out HF/VHF communications [60]. Lower frequency communications, which under normal conditions reflect to the D or E regions, are reflecting to lower

heights and the propagation paths are significantly changing. PCA events can last for days depending on the intensity of the solar proton event. PCA QDCs are in Fig. 2.10, while PCA in Fig. 2.11. A solar flare may last for an hour. A proton event can be observed a few hours after the beginning of the solar flare and can carry on for days. The protons require 1 hour on average to reach the Earth.

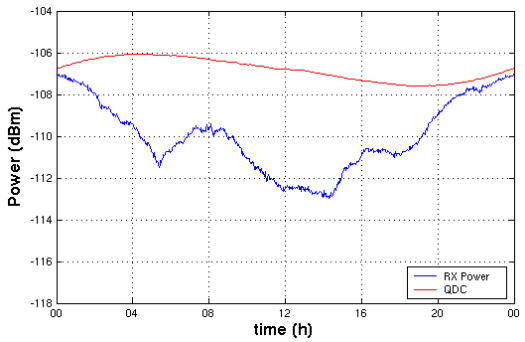


Figure 2.10 QDCs of PCA.

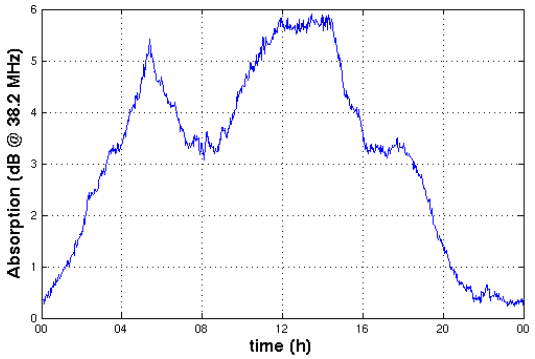


Figure 2.11 PCA.

2.2.3.4 Sudden Ionospheric Disturbances (SIDs)

SIDs are due to random abrupt solar flares [9]. The D region of the day lit hemisphere is highly ionised by an outburst of ultraviolet (UV) radiation from the Sun. CNA increase is observed in the medium and high frequency ranges. SID QDCs are in Fig. 2.12, and the resulting absorption in Fig. 2.13. SID events measure solar activity. There are five taxonomies for the solar activity, noted as levels 1-5 [61]. In level 1 solar activity, there are less than five unexpected quiet regions of the sun. Less than ten class C sub-flares are expected, each corresponding to an X-ray blow with peak flux of 1 to 10 angstrom. The power transmitted is less than 10 mW/m^2.

In the next level, less than ten unexpected quiet regions are observed. Only class C sub-flares are expected. One step upwards, eruptive regions of the sun are observed. Less than five X-ray events are expected. The radiation is classified as class M, with a peak flux of 1-10 angstrom and transmitted power greater than 10 and less than 100 mW/m^2. In level 4, the active regions of the sun are responsible for the SID event. Class M X-ray events can be accompanied by either one or two chromospheric flares.

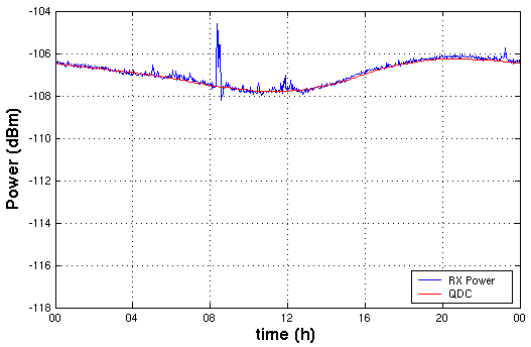


Figure 2.12 QDCs of SIDs.

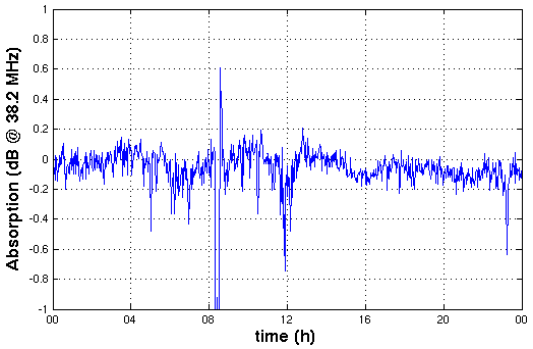


Figure 2.13 SCNA.

Finally, the last scenario contains the highest activity. Protons can be produced in a region on the sun. Class X X-ray burst and several chromospheric flares can occur. Class X X-ray burst corresponds to power transmitted of more than 100 mW/ m^2.

SID events are based on hard X-rays in the range of 1 to 10 Angstrom. Usually, SIDs commence simultaneously or a couple of minutes after the initiation of a solar flare. The duration of a SID is longer than a solar flare. The active high time is faster the fall time. The SID absorption measured by a riometer is also called Sudden CNA (SCNA).

2.2.3.5 Ionospheric Scintillation

CN passing through the ionosphere is subjected to a sudden change of phase and amplitude, called ionospheric scintillation [62]. This is due to the large electron density gradient along the signal path.

The power of strong point sources, such as Cassiopeia and Cygnus, is measured to have large variations. The random change of CN's phase provides a set of different product results. Sometimes they cancel out and the point source is not observed and some other times they multiply the amplitude of the normally expected power. This also called destructive and constructive interference, respectively. Scintillation is plotted in keograms, as in the example of Fig. 2.14.

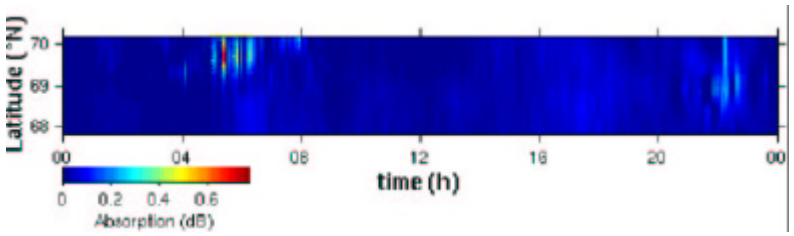


Figure 2.14 Ionospheric Scintillation.

Ionospheric scintillation is not observed by widebeam riometers, due to the long integration time and the resolution of the accumulated results. Only imaging riometers observe scintillation.

2.2.3.6 Solar Radio Emissions (SREs)

The Sun emits centimetric and decametric wavelength radiation. The wavelength of the radiation is related to the Sun's activity. The solar radio emissions are categorised to four taxonomies, based on their wavelength [63].

Category I corresponds to the frequency range 50 - 300 MHz. This emission consists of many narrowband, short in period bursts. Category II commences from 300 MHz and after a period of time progressively reduces to 10 MHz. Category II emissions are slightly associated with major flares. They consist more of an indication that a shock wave is moving through the solar atmosphere.

Category III consists of narrowband bursts that sweep within seconds from decimetre to decametre wavelengths. This corresponds to a frequency sweep from 0.5 to 500 MHz. Practically this category consists of a group of solar emissions and is a measure of the complex solar active region activity. Category IV has a frequency spectrum from 30 to 300 MHz. In this category only broadband bursts are present. These bursts are associated with some major flare events beginning 10 to 20 minutes after the flare maximum, and can last for hours.

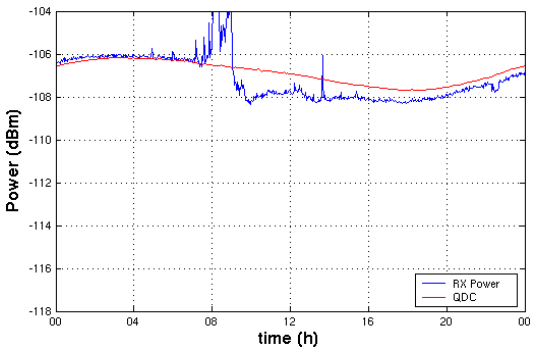


Figure 2.15 QDCs of SRE.

QDCs of SRE are in Fig. 2.15. SREs occur during daylight hours. SREs correspond to an increase in the power results. The SRE absorption is in Fig. 2.16. During a SREs, the increased received power corresponds to a large magnitude negative absorption.

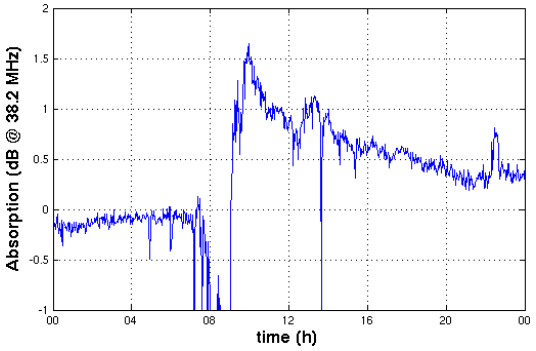


Figure 2.16 SRE Absorption.

The intensity of SREs can cause problems to riometer instrumentations. To the best of our knowledge, all widebeam and phased-array riometers studied so far, cannot measure the full extent of the event. SREs can saturate the receiver's ADC for some time, since the power values are over the range of the receivers.

2.2.3.7 Lightning

Lightning is also observed by a riometer. QDCs for lightning are in Fig. 2.17. The signature on absorption is in Fig. 2.18. A similar signature is left by a sudden, high peak SRE. Experience on data analysis is required to distinguish between lightning and sudden SREs.

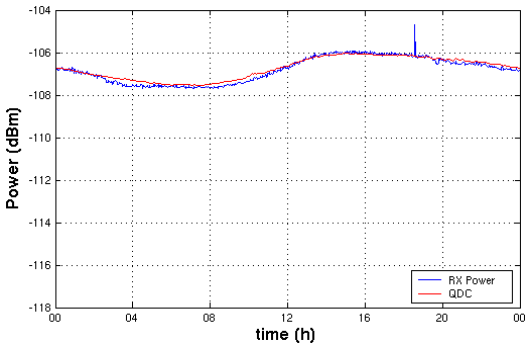


Figure 2.17 QDCs of Lightning.

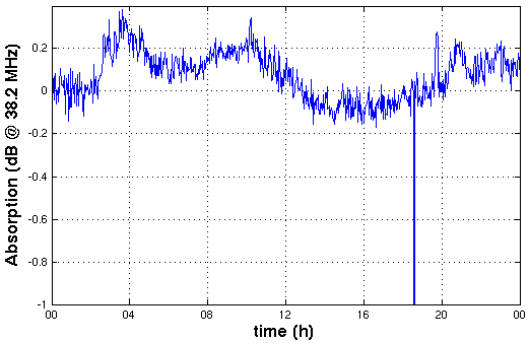


Figure 2.18 Lightning Absorption.

2.2.3.8 Interference

Many riometers are tuned to 38.2 MHz. Although this frequency is reserved for Radio Astronomy, uncontrolled human made interference can exist. Communications between infantry and control stations use HF/VHF frequencies [19]. Both infantry and control stations are mobile so interference is unexpected. This type of interference resembles to category IV SREs, with unpredictable durations. The modulated components of VHF communications can have a significant impact on data.

Similarly to military VHF communications, HF/VHF personal communications or radio broadcasting stations [64] can influence data. As already mentioned, HF/VHF communications, space weather conditions, normal weather conditions with variations in temperature and ground conductivity, the variation of the ionospheric density and ionisation can all influence the reception of CN. The variation of the angle of ionospheric reflection can end HF/VHF communications paths close to the area where riometers are located [60].

Riometers can be affected by car ignition. The motor start of engine vehicles transmits a component of high intensity at the L-VHF. The result would be similar to the frequency response of a lightning or a short and spiky SRE. Riometers are installed in areas where vehicle access is restricted or engine operated equipment with a motor start are not used.

2.3 Magnetometry

The following sections compare existing analogue and digital magnetometers and sensor instrumentations. Conclusions are extracted based on each technology's advantages and disadvantages. The bibliography on magnetometers is plethoric and few major sources are in [62-82]. Emphasis is given to magnetometers with sensors measuring the Earth's magnetic field that are used to study the complex solar wind-magnetospheric-ionospheric system.

2.3.1 The Earth's Magnetic Field

Earth's field magnetometry is described in the major source [83]. A guide for magnetic measurements and observatory practices is published by the International Association of Geomagnetism and Aeronomy (IAGA) [84]. Earth has a crust, mantle and metallic core. Most of the core is liquid and its inner part is solid. Research is under development for the increase of the "frozen" part of the inner core. Along with the Earth's rotation, the magnetic dynamo model is assumed to create the Earth's magnetic field. The north magnetic pole is located roughly 700 miles from the geographical North Pole towards America. It is the south pole of a corresponding dipole magnet, since it attracts the north pole of the magnet needle. The Earth's magnetic field is currently decreasing 0.1% per year, the pole moving to the west by 0.1 deg per year and the tilt of the dipole axis is roughly 10.3 in 2004 [85]. The total intensity of the Earth's isodynamic map on 1/11/2004 is in Fig. 2.19 [167].

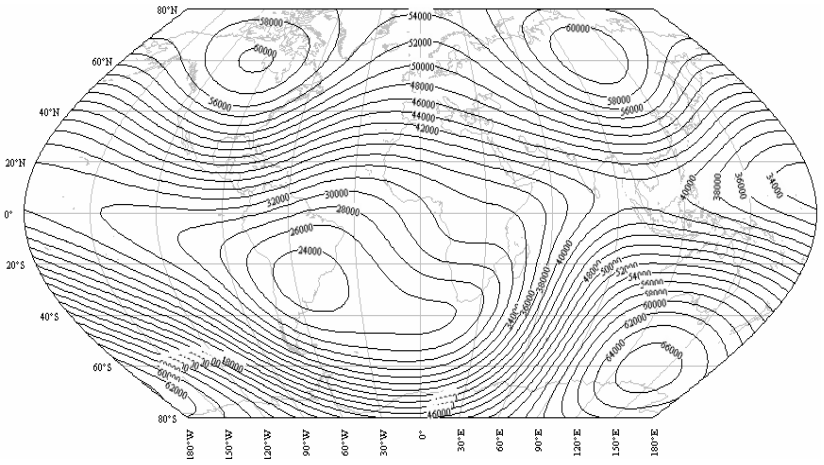


Figure 2.19 Earth's Total Intensity Isodynamic Map for the 1/11/2004.

At the poles the field has a 90-degree inclination and magnitude of 60 uT. At the equator the field has 0 degrees inclination and magnitude of 30 uT. There are anomalous cases where the field is 180 uT vertical (Kursk, Russia) and 360 uT vertical (Kiruna, Sweden). Other anomalies are created due to the magnetisation of the rocks and human ferromagnetic structures that can affect communications. During a day the magnetic field can fluctuate between 10 – 100 nT, due to solar radiation and the induced ionisation of the ionosphere. The observed micro-pulsations have periods of 10 ms – 1 h and amplitudes up to 10 γ. Magnetic storms happen frequently within a month, last for couple of days and exhibit amplitudes of few hundreds of nT.

In geophysical measurements the scalar resonance magnetometers are used. Overhauser magnetometers have replaced the classic proton magnetometers. Optical magnetometers are used for airborne applications. In typical 3-axial vector measurements, fluxgate magnetometers are used.

2.3.2 Sensors Comparative Analysis

There are many categories of sensors [86]. The commonly used and widely available ones are the fluxgate, magneto-optical, giant magnetoimpedance (GMI), magnetoresistor (especially the anisotropic magnetoresistance (AMR)), Hall, induction, superconducting and quantum interference devices (SQUIDs) sensors. There are also some unusual types of sensors that do not belong to any of the above categories.

Unusual means that they are not commercially available or used from some researchers and then got forgotten (e.g. integrated resonant sensor [87]). Most frequently, for a sensor not to be widely available means that there are serious problems with its performance, as for instance the variable inductance thin-film sensors [88]. This is the reason the GMI sensors replaced them. Other not so practical semiconductor sensors, with the exception of the commonly used Hall sensors, are the magnetodiodes, carrier-domain devices and magnetodiodes [89-90].

From the literature, the magneto-optical and GMI sensors are the most recently developed sensors and have many advantages [91]. Measurement of the magnetic fields and electric currents is a standard application for magneto-optics. The measurement is achieved by quantifying the direct influence of external magnetic fields on light. Experimentation is required to determine whether the Earth's magnetic field is capable of affecting the light beam. The cost of building a fibre optics laboratory to test the technique is high. The technique has never been used by ground-based or space-borne magnetometers. It depends on the polarisation rotation due to temperature variation. Regarding the temperature dependence it is hard to distinguish between the change of the external field and the temperature changes. Optical fibres coupled to magnetostrictive material produce a similar sensor type. Tape or wire glued to the fibre acts as the sensor. This technique yields to a complicated and unstable design [92]. Similarly, the sensors categorised as unusual are not recommended due to their limited commercial availability and poor performance. Additionally, although they exist for years they were never used to measure the Earth's magnetic field.

GMI sensors have excellent performance at low price. They are suitable for medical applications, since they follow the control of human physiological functions. They are also used for industrial control and automation. However, they require complex analogue circuits. The miniature technology requires extra cost for familiarisation and a budget for laboratory equipment. Another concern is that their high sensitivity ($B \approx 10$ fT) is unsuitable for measuring the Earth's magnetic field ($B \approx 60$ uT).

Low-temperature SQUID sensors are used in case pT or smaller fields are to be measured. Fluxgate and SQUID sensors have similar noise levels, however fluxgates have larger dynamic range. The AMR sensors exhibit worse resolution of more than 10 nT, but they are smaller and consume less power than fluxgates. Similar to riometer systems, dynamic range and resolution is a crucial design factor, which biases the selection process. The analysis mutually excludes most of the sensors and leaves fluxgate sensors as the suitable candidate. If a deep space application was intended, then the AMR sensors would have been considered for their size and power consumption.

2.3.3 Fluxgate Sensors

Fluxgate sensors measure the magnitude and direction of the dc or low frequency ac magnetic field in the range of 10^{-10} to 10^{-4} T. An ac excitation field of frequency f through the excitation coil drives the soft magnetic core to saturation, as shown in Fig. 2.20. The core permeability changes with 2f frequency and the dc flux $\Phi(t)$ is modulated. Flux is derived from the external dc magnetic field Bo. An induced voltage proportional to Bo at the second and higher even harmonics of the excitation frequency is measured at the measuring coil of N turns [93].

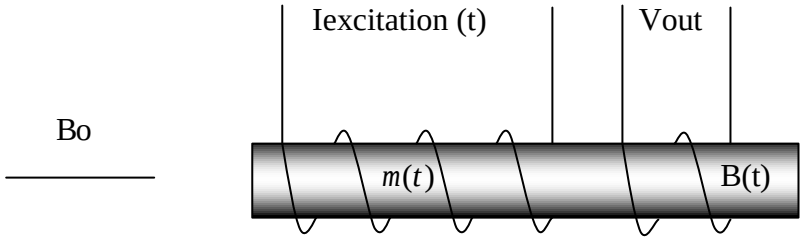
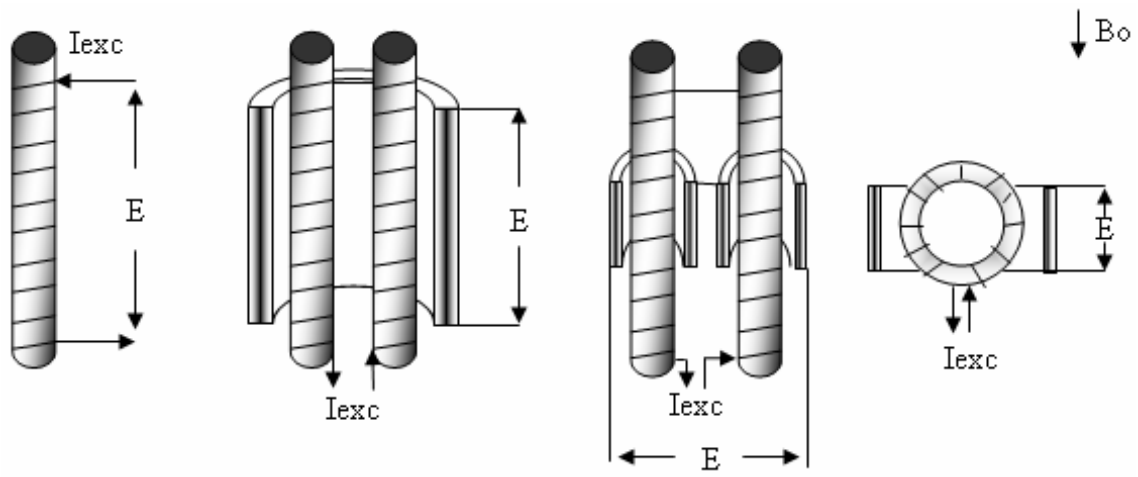


Figure 2.20 The Fluxgate Principle using a Parallel Type Sensor.

The work on fluxgate sensors started from the late 1920s and the first patent was granted in 1931 [94]. Fluxgate sensors have been used on the Moon and in deep space [95]. They are solid-state devices with no moving parts and can work under different temperatures. Commercial products have roughly resolution and absolute precision of 100 pT and 10 nT, respectively. They operate between several Hz up to kHz. A drift of 0.1 nT/$^\circ$C and a sensitivity coefficient up to 1 ppm/$^\circ$C in certain cases prove their stability with temperature. A typical linearity is 30 ppm.

The first category of fluxgates to be examined is the orthogonal type sensors. As the name implies, the excitation field is perpendicular to the sensitive axis of the sensor. The pioneer of this type is Alldredge [96] and the sensor has a core of a ferromagnetic wire or a tube. A current excites the core in the first type, however the disadvantage is that at the core centre the excitation field is zero, which affects the sensor remanence. The tube type is excited by one wire in the tube [97]. A helically wounded tape on a tube forms an orthogonal-parallel sensor [98].

Parallel type sensors have better performance and are more suitable for a low-noise fluxgate. For a low-noise precision fluxgate the ring-core parallel type or double-rod sensors are investigated. The major parallel type fluxgates are in Fig. 2.21. The single core sensor of Fig. 2.21 (a) is used for undemanding applications [99]. The disadvantage is that it acts as a transformer, since a large signal at Fexc and odd harmonics is produced at the sensor's output. The problem is solved using a double-core sensor as in Fig. 9.3 (b). The two parallel excitation cores are excited in opposite directions to nullify the mutual inductance between the sensing and excitation coils [10]. The two serially connected excitation coils of Fig. 2.21 (c) permit flexible matching and sensor balancing by moving the excitation coils with respect to their sensing coils [101].



a) b) c) d)

Figure 2.21 Fluxgate Parallel Type Sensors.

Configurations b) and c) present increased sensitivity, directivity and resistance to orthogonal fields. However, open-ended rods have a higher noise figure, vulnerability to perming effects and temperature offset drifts, difficulty in saturation and high power consumption.

Race track sensors are closed-type sensors made from sheets in the shape of circular or oval flat rings. They have a lower demagnetisation factor, higher directional sensitivity, less sensitivity to orthogonal fields (interference) [102]. A race-track sensor of etched sheets and an 8 layer 35 um thick amorphous ($Co_{67}Fe_4Cr_7Si_8B_{14}$) core is presented in [103]. The disadvantages of race-track sensors are the large

spurious signals, which are impossible to balance them as the ring-cores can, and potential problems from higher tape pressure in the corners. On the other hand, ring-core sensors have an anuloid excitation coil and a solenoid-sensing coil, as shown in Fig. 2.21 (d). The core consists of several turns of soft magnetic material thin tape. Although they have low sensitivity due to the demagnetisation, ring-core designs have many advantages and produce low-noise sensors. Rotating the core with respect to the sensing coil permits precision balancing of the core symmetry. Ring-core sensors exhibit uniform distribution of any mechanical stress. The increased noise associated with open-ended rods is absent. Tape ends are an insignificant source of noise. Sensitivity is proportional to the sensor diameter. For a given diameter, a trial-by-error procedure determines the optimum for the other dimensions.

2.3.4 Analogue Magnetometers

A review on fluxgates is in [93]. Detailed instructions for a basic fluxgate are in [104]. The major components of the second harmonic fluxgate magnetometer are shown in the block diagram of Fig. 2.22.

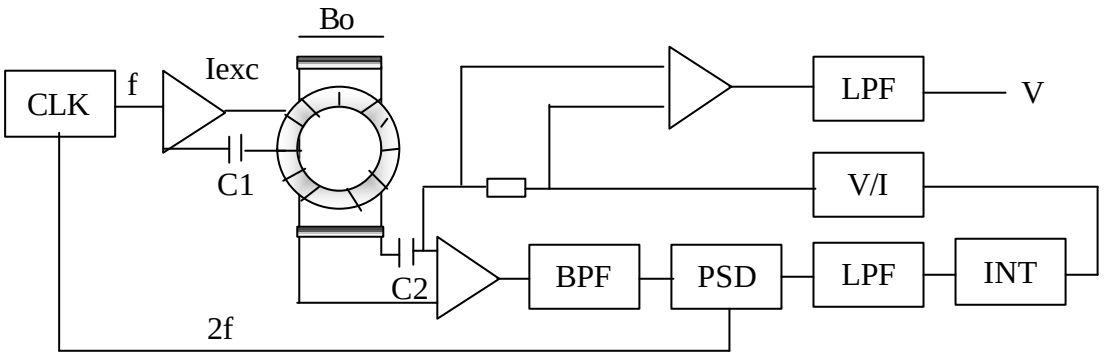


Figure 2.22 2nd Harmonic Fluxgate Magnetometer Block Diagram.

A frequency generator generates the f and 2f frequencies. The f frequency is a sine-wave or a square-wave between 400 Hz – 100 KHz and excites the sensor. For crystalline core materials a 5 KHz square-wave is used. The power amplifier is a totem-pole pair of hexfet transistors. The 2f signal switches the phase-sensitive detector (PSD). The sensor output is amplitude modulated by the Earth's magnetic field and the PSD demodulates it to dc. The analogue feedback has a large gain, so the sensor functions as a zero indicator. The current output of the voltage-to-current (V/I)

converter increases the dynamic range of the instrument and is the current into the compensation coil. The feedback gain controls the sensor's nonlinearity and sensitivity. The sensor coil has roughly 2000 turns. Pre-amplification and bandpass filtering prior to PSD filters the first harmonic and other spurious signals at the sensor's output. The integrator provides sufficient amplification.

A low-power two-axis analogue magnetometer for vehicle detection is in [76]. The system demonstrated a significant temperature offset drift of 6 uT in the -40 deg C to +70 deg C range. The offset drift was reducing by increasing the power consumption. A tri-axial analogue fluxgate magnetometer is in [77]. The system has a large power consumption of 300 mW, compared to the 5 mW of the system in [76], a range of +/- 100 uT with 1 nT resolution.

A single-axis and a proton magnetometer measure absolute values. Because both systems are mounted on top of a theodolite telescope this technique is called fluxgate theodolite. It measures the magnetic declination D and inclination I, as explained in [72]. A similar instrument is in [73].

Three-axis magnetometers record magnetic variations and they rely on the temperature stability over long periods of operation. Calibration routines by absolute measurements reduce the absolute error to 1 nT. Comparisons of different magnetometers were performed at workshops [74-75]. Observatory fluxgate magnetometers are made by GEM, EDA, Narod Geophysics, Dowtry, Scintrex, Thomson-Sintra, Shimadzu [82] and others.

2.3.5 Digital Magnetometers

Certain authors claim that digitisation of analogue magnetometers is unnecessary, since there is no improved performance apart from the simplification of the circuit [105], however, recent developments have proved quite the opposite.

The first digital fluxgate magnetometer is presented in [65], verifying that digital technology can be employed into magnetometry. The first real-time fluxgate magnetometer using FPGAs was made by MPI [66].

A digital fluxgate magnetometer was added to the instrumentation of the Swedish satellite Astrid 2 [68]. Another solution is presented by Kawahito et al. [69-70]. An analogue switching type synchronous detector was used connecting to an analogue integrator and a second order delta sigma modulator. A one-bit digital-to-analogue converter (DAC) was used to close the magnetic feedback loop. The 1-bit DAC guarantees linearity. The output of the DAC is connected to an analogue low-pass filter (LPF). The system's disadvantage is the excessive noise of the device, because the magnetic circuit was implemented in the same device with the digital signal processing electronics.

The solution in [106] implements the system, apart from the sensor, into a single chip using mixed logic. However, the cost of the required software, manufacturing processes cost and design time leaves this idea for future reference.

Chiezi integrated high-performance amorphous ferromagnetic ribbons on silicon wafers using complementary metal-oxide semiconductor (CMOS) manufacturing techniques and batch integration post-process of the ferromagnetic cores to create a 2-D fluxgate for electronic compass applications. The two cores are placed diagonally above the single square driving coil and the sensor is equivalent to a parallel type. However, the significant error of 1.5° (0.5 uT) makes the system inaccurate even for electronic compass applications.

Space physics, amongst others, is dedicated to the precise measurement of the ambient magnetic field's total intensity. The results from space missions are in the range of 5 pT – 2 mT, with a typical accuracy of 1°. High accuracy is required for mapping of planetary magnetic fields. The integration time for the correlated data is from 1 s to hundreds of samples per second [107]. Most magnetometers are of the vector type. Scalar magnetometers measure only the magnitude the ambient field, not the direction and, therefore, are not suitable for this study. A review of space magnetometers is in [108].

Rockets and balloons also measure the Earth's magnetic field, the equatorial electrojet strength, the auroral current system and other high-altitude magnetic phenomena. In 1940's, space probes discovered the morphology of the magnetosphere. Space missions determine the magnetic fields of most of the solar system planets, the interplanetary medium, comets and asteroids. Currents driven by thermal convection between their mantles and liquid metallic cores create the Earth's magnetic field. The same applies for Jupiter and Saturn, but not for the other planets. Magnetic field measurement is used in spacecraft attitude determination and control, orientation, momentum management and scientific instrument pointing. Additionally, it assists the study of plasmas in the solar system and the behaviour of energetic trapped particles around magnetised planets.

Vector magnetometers are the most widely used instruments on balloons, sounding rockets and spacecrafts. They provide measurements of the field strength, direction and ambient field. Tri-axial systems are usually implemented. The calibration process is based on known magnetic fields both in amplitude and phase. The specifications include their output for zero-field, scale factor, temperature stability, time drift, weight, power consumption, operating temperature range and radiation hardness. The Earth's magnetic field has been mapped using vector magnetometers with a resolution of 5 nT and 3 arc-seconds [109-110].

2.3.6 Ground Based Magnetometer Networks

Ground based magnetometers couple the operation of space born systems. They assist in quantifying geomagnetic events and measuring the Earth's magnetic field. It is obvious that the field of magnetometry has been developing at a fast pace and advanced networks of magnetometers have already been in operation for many years. An introduction is given to the most important networks in existence, such as the INTERMAGNET, EISCAT, SAMNET and IMAGE networks. The information that can be extracted from the study of these networks is the available magnetometer types, specifications and inspiration to create a novel ground based digital magnetometer.

The International Real-time Magnetic Observatory Network (INTERMAGNET) is a global network of magnetic observatories, measuring the Earth's magnetic field [111]. An INTERMAGNET Magnetic Observatory (IMO) provides 1 min magnetic field values at 0.1 nT resolution from a vector and an optional scalar magnetometer. An IMO must comply with the specifications of Tables 2-1 and 2-2.

Resolution:	0.1 nT
Dynamic Range:	6000 nT Auroral & Equatorial, 2000 nT Mid Latitude
Band Pass:	DC to 0.1 Hz
Sampling Rate:	.2 Hz (5 sec)
Thermal Stability:	.25 nT/°C
Long Term stability:	5 nT/year
Accuracy:	±10 nT for 95% of Reported data, ±5 nT for Definitive data

Table 2-1. IMO Vector Magnetometer Minimum Requirements.

Resolution:	0.1 nT
Sampling Rate:	0.033 Hz (30 sec)
Accuracy:	1 nT

Table 2-2. IMO Scalar Magnetometer Minimum Requirements.

Vector magnetometers include: EOPGS DI-Flux Mag 93, GEOMAG MV390, MAG-01H, LEMI-008, ELSEC 810, Narod ring core, 3-D parallel core etc. Scalar magnetometers: Overhauser, Proton Precession PM587, G-856, GM122, PMP-7 etc.

The EISCAT magnetometer cross [112-113] was operating between 1982 and 1991. At maximum, seven digital tri-axial fluxgate magnetometer stations operated since summer 1983. These stations were located at Alta, Kevo, Kilpisjarvi, Kautokeino, Muonio, Pello and Soroya. The sampling period and the magnetic field resolution were 20 s and 1 nT, respectively. The EISCAT cross was a German-Finnish collaboration, directed by the Technical University of Braunschweig. The IMAGE magnetometer network is considered to be an expansion of the EISCAT cross.

The International Monitor for Auroral Geomagnetic Effects (IMAGE) consists of 28 magnetometers from 10 institutes from Estonia, Finland, Germany, Norway, Poland, Russia and Sweden [114]. Due to its 58 to 79 degrees variation of latitudes, IMAGE studies long-term geomagnetic activity, auroral electrojets and two-dimensional current systems [115]. Joint experiments with radars, riometers, all-sky cameras and satellite instrumentations investigate high-latitude magnetospheric-ionospheric physics. The time resolution is 10 s.

The Sub-Auroral Magnetometer Network (SAMNET), operated by Lancaster University, consists of 13 tri-axial analogue fluxgate magnetometer stations. They use the double-rod parallel type sensors, encapsulated into epoxy material for temperature stability, mechanical stress relief and maintenance of the sensors orthogonal relation.

Since 1987, the participating stations are in the UK (Crooktree, Eskdalemuir, Glenmore Lodge, Hartland, Lerwick and York), Faroe Islands, Sweden (Kvistaberg and Uppsala), Norway (Nordli), Finland (Hankasalmi, Kilpisjarvi, Nurmijarvi, Oulu and Oulujarvi), Iceland (Borok and Hella) and Russia. SAMNET incorporates data from 3 British Geological Survey (BGS) magnetometers. Typical measurements of SAMNET include the determination of Pi2 pulsations [116-117]. The time resolution was initially 5 s and for the last 10 years 1 s.

2.4 Digital Systems Design Techniques

The following sections address the different hardware (HW) and software (SW) techniques that can implement the digital riometer and magnetometer systems. A digital HW design is a combination of different digital building blocks. It includes general-purpose processors, ASICs, DSPs, FPGAs, multi-processors, digital filters, ADCs, DACs, memory, digital interconnect, storage etc. A digital HW architecture is characterised by a reference platform. A reference platform stipulates a basic set of specifications that the new riometer and magnetometer designs have to comply before their development commences. The major technical aspects of the available architectures are analysed and by means of comparison their tradeoffs are extracted.

The design methodology to be followed for the two new systems has a profound impact on both the effort consumed and the outcome of these designs. Apart from the actual HW development other design strategies have to be incorporated, such as SW engineering, to form a synectic set of specifications increasing the possibility of two successful designs. While the general design methodologies have not changed over a long period of time, the design styles have blossomed alongside technological advancements and productivity levels.

Each system is defined by three hierarchical high-level design abstraction layers, namely functional, morphological and physical. Functionality defines the system's top-level behaviour, e.g. a programmable and dynamically reconfigurable riometer for CNA measurements. Morphology defines the subsystems' connections to realise functionality, e.g. the riometer consists of a broadbeam antenna, an RF receiver, a central processor unit (CPU) and software all interconnected appropriately. The physical layer corresponds to subsystem design, including component-level, analogue and digital schematic circuits.

The different layers are associated with each other, as shown in Fig. 2.23, where the original Gajski Y chart [118] has been customised for the needs of the thesis. The three radial lines represent the functional, morphological and physical layers. The outer shells of the chart represent complex systems, such as the riometer and magnetometer. Circles represent sub-layers of similar abstraction.

The functional layer encompasses standard SW and HW description languages (HDLs). HDL based systems implement DSP algorithms (alg.) using register transfer logic (RTL) that contains logic gates (Logic) expressed by actual HDL statements (Stat.). The instruction set architecture (ISA) provides the critical interface between HW and SW. It is being called by routines within a program (Prog.) as part of a SW application (App.) running on a variety of operating systems (OSs).

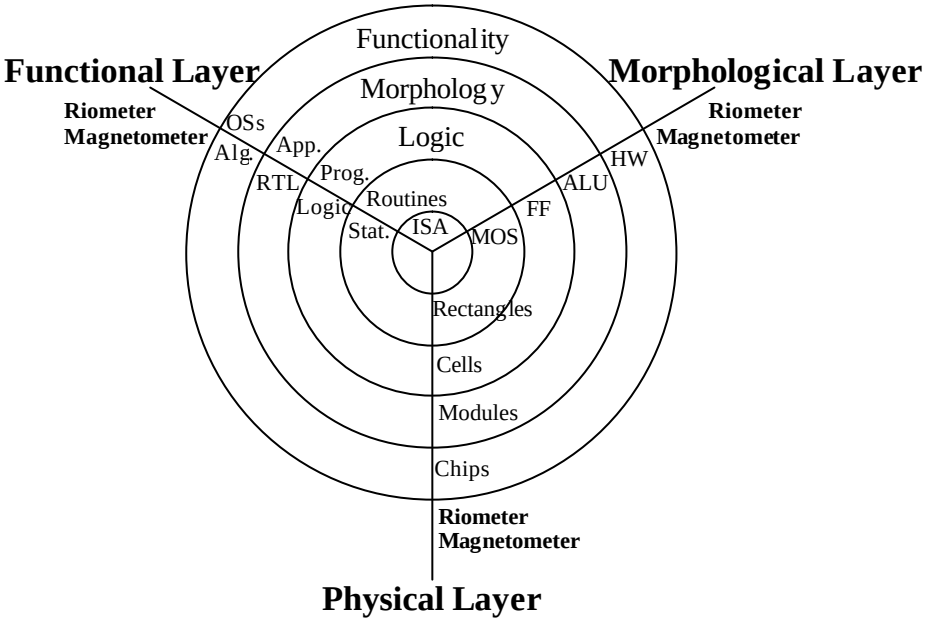


Figure 2.23 Modified Gajski Y Chart.

ISA is reprogramming and reconfiguring the state of transistors (standard nMOS and pMOS in rectangular layouts within the floorplan) that connect to create logic cells representing synchronous flip-flops (FFs) and asynchronous gates. These building blocks create arithmetic and logic units (ALUs), datapaths, controllers, memories etc. and can be found on the different HW modules that the two systems would be built on. At the top-level, ISA is controlling the physical-layer ICs on the systems' PCBs.

The life of the two systems depends on the usage and productivity of the designs. This depends on how efficiently the projects will be converted from theory to practice. Analysis is required to conclude on some important parameters such as performance, size, cost, design time and verification. It is inefficacious to pursue an expensive custom VLSI design when off-the-shelf components exist fulfilling the systems specifications at a lower cost. Microprocessors and DSPs are examined first.

2.4.1 Microprocessors and DSPs

Many practical systems use a microprocessor (uP) or a DSP. Most uPs have embedded ROM, RAM, EPROM or Flash ROM. For instance, Microchip Technology produces 8/16-bits PIC uP families. DSPIC33FJ256G710 is one of the high-end PIC uPs with CPU speed of 40 MIPS, 256 KB program Flash, 30 KB RAM, 85 I/O on a 100 pin device, 12-bits ADC at 500 KSPS etc. PIC uPs are suitable for motor control, industrial, surveillance and other low-frequency applications where DSP is minimum. For mathematically intensive operations DSPs are preferred. Texas Instruments (TI), founded in 1941, is the leader in DSPs. Analog Devices (AD) manufactures DSPs, but it specialises more in multimedia processors such as DACs, codecs, filters etc.

TI's DSPs have been extensively used in the 80's and 90's replacing analogue hardwired systems and creating new ones [119]. The 16-bit fixed-point TMS32010 with external memory (1983) is the world's first DSP, of the popular TMS320C1x family. TMS320M10 is the same DSP with internal 3 KB ROM. The TMS320 family consists of generations of DSPs with several devices in each generation. DSPs were split between fixed-point and floating-point devices to increase the accuracy of real-time applications. Floating-point DSPs are used by scientific applications where extra range precision is more important than speed. The C3x (e.g. TMS320C33) and C4x families include floating-point DSPs, while the C2x and C5x [120] fixed-point. C6x includes both fixed-point (C62x and C64x) and floating-point (C67x) DSPs. DSPs influenced general purpose CPUs, e.g. Intel IA-32 ISA added MMX extensions [121].

The first DSPs (C1x, C3x) focused on the multiply and add function. Later designs supported improved specifications and a flexible I/O scheme. A core is an ISA embedded into the DSP. Intellectual property issues arise from embedded cores and other commercial circuits into the same DSP [122]. For the wireless market Motorola produced the DSP56304 built on the DSP56300 core. Other cores include ADSP 21xx SHARC (400 MHz/2400 MFLOPS) [123]. Star Core [124], the Oak/DSP Group, Advanced RISC Machines and other companies are core suppliers. The competition between RISC machines and Intel's IA-64 Merced is in [125]. DSP technology is constantly developing as research yielded to interesting commercial products [126-127].

DSP systems are reprogrammable without HW modifications and perform functions not possible with analogue circuits. They can be updated on site with software patches. High-level languages like C/C++ are used to program the devices. DSPs are unconditionally accurate, as accuracy is only determined by the number of bits used on the internal busses. The performance from device to device is identical since the tolerance of the components is the same. There is no temperature drift. DSPs feature high reliability, low power consumption and high speed. DSPs are used in aerospace, military, digital filtering, audio, image and video processing, control etc.

However, the cost and time of software development can be unexpectedly high for uP/DSP systems. Parallel processing is event driven and is based on the sequential execution of commands within software loops. Building a system with an off-the-shelf DSP may yield to a successful design and the possibility of seriatim integration should be considered for mass productions. It is cost effective to embed the uP/DSP and various peripheral chips into a single-chip. Therefore, a uP/DSP should be considered before the commencement of the design that can be embedded so the same software can be reused. For instance, other processor cores from the ones already mentioned include MIPS, ARM and IBM's PowerPC. The Sun Microsystems SPARC V8 is available in VHDL from Gaisler Research.

2.4.2 Programmable Design Techniques

A wide range of programmable chips is available which can be more efficient than uPs and faster to develop than dedicated chips or DSPs. These can be devices with programmable logic arrays, programmable interconnect and reprogrammable logic and interconnect. These techniques yield to modular designs, where each aspect of the design is considered independently. Solutions are provided at the IC level and parameters such as maximum frequency of operation, cost, development time etc. are more sufficiently optimised. Both reprogrammable and reconfigurable at the physical layer systems are produced in this way. It is important to clarify that general purpose CPUs, uPs and DSPs are only software reprogrammable and not HW reconfigurable, since their physical layer architecture is fixed. Reprogrammable and reconfigurable systems can implement a wider range of applications using the same hardware.

2.4.2.1 Programmable Logic Devices

The programmable logic array (PLA) [128] logic device consists of a programmable AND array connected to a programmable OR array. The outputs may also be programmed to give a true or complement output. These devices can implement two-level sum-of-product expressions and to replace combinational logic circuits used in control and decode applications. A floating-gate transistor, a fusible Ni-CA link or a RAM-controlled transistor is used to program the device. The first two methods were used when device densities used to be low, but currently the third method is preferred for reprogrammable solutions. However, PLAs have limited routing capability and small gate capacities compared to the FPGAs described in the next section.

2.4.3 Field Programmable Gate Arrays (FPGAs)

An FPGA is a block of programmable logic that can implement multi-level logic functions. Each FPGA is reconfigured and reprogrammed by the designer at his site. They differ from mask-programmed gate arrays, as no IC masking steps are required. Being off-the-shelf parts, FPGAs can be programmed and tested as soon as the design is completed. Xilinx [129] has been the leading FPGA manufacturer since its establishment in 1984. Companies such as Altera, Lattice, Actel etc. follow both in net revenues, market shares and technology evolution (e.g. 10 um in 1971 for Intel's 4004 CPU, 0.6 um in 1994 and 65 nm in 2006 for Xilinx Virtex-5 and Intel's Core 2).

In 1984, Xilinx introduced the XC2000 family and in 1985 XC2064 (<1500 gates) was the world's first commercially available FPGA. In 1984 its major competitor, Altera, was founded. The CMOS UV-EPROM technology was introduced at the same year. Xilinx was expanding for a couple of years and in 1991 launches the XC4000 family. In 1992, Altera launched its first FPGA Flex 8000 (<15,000 gates). In 1993 the EEPROM technology was introduced. In 1998, Xilinx introduced the Virtex family (2.5 V core voltage, 0.22 um process). In 1999, the (1.8 V, 0.18 um) Virtex-E and the low-cost CoolRunner complex programmable logic device (CPLD) family. In 2000 the Virtex-EM (1.8 V, 0.18 um). In 2001, Xilinx introduced the Virtex-II family (<10 million gates, 1.5 V, 0.15/0.12 um) and Virtex-II Pro (<99,216 logic cells (LCs), 1.5 V, 130 nm) with two embedded 32-bit IBM RISC PowerPC 405 uPs, up to twenty

3.125 Gbps RocketIO tranceivers (XCE2VP100FF1704 with 1040 I/Os) and up to 1164 user I/Os (XCE2VP100FF1696 with 0 RocketIO). In 2003, Xilinx introduced the low-cost and high density Spartan - 3 family (<5 million gates, 1.2 V, 90 nm).

In 2004, Xilinx released the Virtex-4 family (<200,448 LCs, 1.2 V, 90 nm, 500 MHz) shortly to be named product of the year, according to the Electronic Products Magazine. The Virtex-4 family offers three platforms and 17 devices in total to allow the development of a variety of applications. The LX platform provides the highest number of LCs (200,448) and user I/Os (960 for XCE4LX200FF1513), the SX platform the highest number of DSP and embedded memory features (55,296 LCs, 5,760 Kb BRAM, 8 DCMs, 4 PMCDs, 512 XtremeDSP slices and 640 user I/Os for XCE4VSX55FF1148) and the FX platform is suitable for embedded processing and high-speed serial connectivity (142,128 LCs, 9,936 Kb BRAM, 20 DCMs, 8 PMCDs, 192 XtremeDSP slices, 2 32-bit IBM RISC PowerPC 405 uPs, 4 10/100/1000 Ethernet MACs, 24 RocketIOs and 896 user I/Os for the XCE4VFX140FF1517).

The 65 nm lithographic process is currently the most advanced technique for massively producing CMOS VLSI designs. Intel implemented this process first and products such as Prescott (1/2006), Pentium 4 (Cedar Mill) [130], Pentium D (900 series), Core, Core 2, Xeon etc. have been announced or already entered the market. AMD announced the Athlon 64X2, while Sun the UltraSparc 2. IBM is expected to use this process for the creation of the Cell Broadband Engine for the Sony Playstation 3. TI, Motorola and Cypress Semiconductor are in the planning process.

The only FPGA manufacturer that entered the 65 nm manufacturing process, as in 5/2006, is Xilinx by introducing the Virtex-5 family [131] (<12 million gates, 1.1 billion transistors, <550 MHz). Virtex-5 also offers three development platforms. The LX platform is optimised for high-performance logic (331,776 LCs, 10,368 Kb BRAM, 12 DCMs, 6 PMCDs and 1200 user I/Os for XC5LVX330-1FFG1760CES). The LXT platform is for high-performance logic with low-power serial connectivity (331,776 LCs, 11,664 Kb BRAM, 12 DCMs, 6 PMCDs, 960 user I/Os, 24 RocketIO tranceivers, 4 x 10/100/1000 Mbps MAC blocks and 1 PCI-X block for XCE5LVX330T-1FFG1738CES). The SXT platform is optimised for DSP and memory-intensive applications with low serial connectivity (94,208 LCs, 8,784 Kb

BRAM, 12 DCMs, 6 PMCDs, 640 user I/Os, 16 RocketIOs, 4 x 1 Gbps MAC blocks and 1 PCI-X block for XCE5VSX95T-FF1136). The cost per device ranges between $220 for the lowest-range XC5VLX30-1FF324CES, rising to $7,683 for the high-end XC5LVX330-1FFG1760CES and $11,597 for the top-performance XC5LVX330T-1FFG1738CES.

Although this technology was recently introduced, developers such as Intel, AMD, IBM, Infineon, Samsung etc. have already planned productions on the 45 nm process for 2007-2008. Intel has already demonstrated Penryn, the next generation of Core 2 CPUs. Xilinx is in discussions with Toshiba and UMC for the next generation of 45 nm FPGAs. Current research on the 32 nm process will conclude to commercial products in 2009-2010. Similarly, the 22 nm and 16 nm processes are under consideration, e. g. 16 nm is expected near 2018 and the earliest is 2013 [132].

2.4.3.1 The Xilinx VHDL Design Flow

The VHDL design flow has remained the same over the years and consists of the design entry, synthesis, functional simulation, implementation, timing simulation and time-based analysis verification, and device programming.

The design entry using VHDL can be achieved by three different means [133]. The VHDL code can be entered directly using the HDL text editor. The state machine editor provides a more graphical approach to design state machines and automatically outputs the required VHDL code. The schematic editor can visualise the interconnections between VHDL modules, in the form of instantiated schematic macros, compiled in the project library.

Unlike other languages, VHDL designs are not synthesised within the HDL editor [134]. The synthesis tools translate the design into a gate netlist, known as EDIF netlist file, which is optimised for a specific FPGA target architecture. Pre-implementation constraint editing, cross-boundary optimisation and auto I/O buffer insertion are only available in the HDL flow project.

The global synthesis options allow setting the default clock frequency, export timing constraints to the place and route software, input XNF bus style, FSM encoding (One-Hot or Binary) and FSM synthesis style. For FPGAs the FSM encoding style is set to One-Hot for best results. The timing and pin location constraints are entered after the elaboration step and are automatically exported to the place and route tools.

For VHDL designs, functional simulation is performed to verify the design methodology, after the design is being synthesised and before design implementation. The circuit's logical operation is examined independent of timing considerations. Gate delays and other timing parameters are considered to be zero.

The implementation process translates, maps, places and routes the design. A downloadable .bit file is created [135]. Translation converts the EDIF netlist to an internal netlist format and rule checks are performed. The mapping stage optimises the design to increase the speed and decrease the number of gates used.

The place and route process assigns the gates in the netlist to specific CLBs and their interconnections are routed through the PSMs and other FPGA routing resources. The timing stage computes the propagation delays through the CLBs and the routing PSMs and stores them in a file for use during the timing simulation. Finally, during the configuration stage a downloadable stream of bits is generated to configure the FPGA to perform the logic functions described in the VHDL file.

Timing simulation is performed after implementation [135]. Timing simulation is more accurate than functional simulation. It verifies that the design runs at the desired speed under worst-case conditions. Timing simulation examines the circuit's operation including estimated delays and ensures that the setup, hold and other timing considerations for sequential devices like flip-flops are met.

Downloading refers to the process of FPGA reconfiguration [136]. The Bit file is downloaded to the FPGA. The configuration data can be verified using an XChecker cable. Verification reads the configuration data and compares it to the original bitstream, ensuring that the device correctly receives the design. Debugging consists of reading the internal FPGA states to verify the design is functioning correctly.

2.4.4 FPGA Architectures

There are three main FPGA architectures:

1. SRAM (Static RAM) based
2. Anti-fuse based
3. Floating-gate technology

SRAM based FPGAs are configured every time the device is powered on. The 'fuse' configuration is held in a configuration Serial Memory along side the FPGA or is held in a co-processor. It is loaded into the FPGA on power up using an algorithm held within the FPGA. SRAM technology leads to clever methodologies like FPGA configuration on the fly.

In the floating-gate technology the FPGA can be programmed with any desired link configuration, as well as erased to its original state, either by applying an electric voltage (EEPROM technology) or by exposing it to ultraviolet light (EPROM technology). In the original, manufactured state, the floating gate has no charge on it and has no effect on circuit operation. In this state, all configurable logic blocks are effectively connected and there is a logical link present at every net cross-point [137].

The main disadvantage of SRAM and floating-gate architectures is security. The configuration bit stream can be read as it configures the FPGA and designs can be copied. Anti-fuse FPGAs on the other hand are single shot devices and are very secure. The device is programmed, by 'blowing' the internal fuses. Once the device is programmed it cannot be reprogrammed. Obviously, there is a certain amount of device wastage in the design phase if the design is not right first time.

If an FPGA design is mature, not likely to change and being used in quite large volumes it may be worth converting to a Gate Array. This conversion service is offered by most of the silicon vendors. It will save money if production quantities are sufficient to offset the None Recurring Engineering (NRE) charge. This process is also making the design secure [138].

2.4.5 Advantages of VHDL

Based on the introduction of Hardware Description Languages (HDL), researchers and hardware designers have developed new digital system CAD tools. The United States Department of Defence (DoD) and IEEE, as part of its Very-High Speed Integrated Circuit (VHSIC) program, developed VHSIC HDL (VHDL) in the early 1980's. VHDL is a powerful general-purpose high-level programming language, similar in style and syntax to modern programming languages, as well as being a hardware description language.

With VHDL is possible to create simulation programs ranging in abstraction from gate-level to system. The universal compatibility between existing CAD tools, in conjunction with the wide choice of hardware implementation targets, allows fast development and short market time. VHDL provides a versatile reusable design module (a digital core) that allows the reuse of the design. Systems consisting of many circuit boards and associated hardware can now be replaced by 'on-the-silicon' design.

VHDL has many features important to accurate hardware simulation. It supports concurrency, which simplifies the description of parallel, connected machines on a chip. It allows precise modelling of delays and other time behaviour. General-purpose programming languages do not provide event-driven scheduling facilities [139].

Chapter 3.
Hardware Design of a Dual-Channel Cross-Correlator System

3.1 Introduction

The chapter is dedicated to the hardware design of a dual-channel cross-correlator. The hardware correlator is seriatim incorporated into the Priamos and Dimagoras systems. Investigation of antenna array theory assists in deriving the required autocorrelation and cross-correlation functions to be modelled in hardware.

In every radio interferometer system, the main DSP function is the correlator. CN may contains partially correlated signals from a partially resolved source. An 8-phase auto-switching dual-channel correlator and a free-input dual-channel correlator are designed. The designs implement the cross-correlation function for non-identical incoming signals.

The designs are hardware implemented using the Xilinx Virtex-II 2V6000 FPGA ADM XRC-II board [140] and the ADC-PMC carrier board. Data are transferred to host via the 32-bits/33 MHz PCI interface.

3.2 Auto-Correlation in Riometry

The theory of phased-array systems is an extension of the analysis used for an array of two antennas, as in Fig. 3.1. Usually after each antenna there is a pre-amplifier. It ensures that subsequent losses through the rest of the system do not affect the quality of the wanted signal. Especially in the riometer case, due to the weak power levels of CN, the usage of amplifiers is essential.

The delay circuit is implemented using transmission lines of different lengths. When phase switching is required in order to produce images by scanning the sky, complex time delay instruments are built, such as butler matrices [30]. In Fig. 3.1, two antennas are connected to two amplifiers. A time delay is inserted at the output of one antenna, such as the arrival delay of the CN wavefront is the same for both antennas. The correlator receives coherent parts of the same signal at each frequency-sampling clock. The correlator performs two mathematical operations: complex number multiplication and integration of the results over a predetermined period of time. The integration time depends on the antenna-array structure and bandwidth of the receiving system.

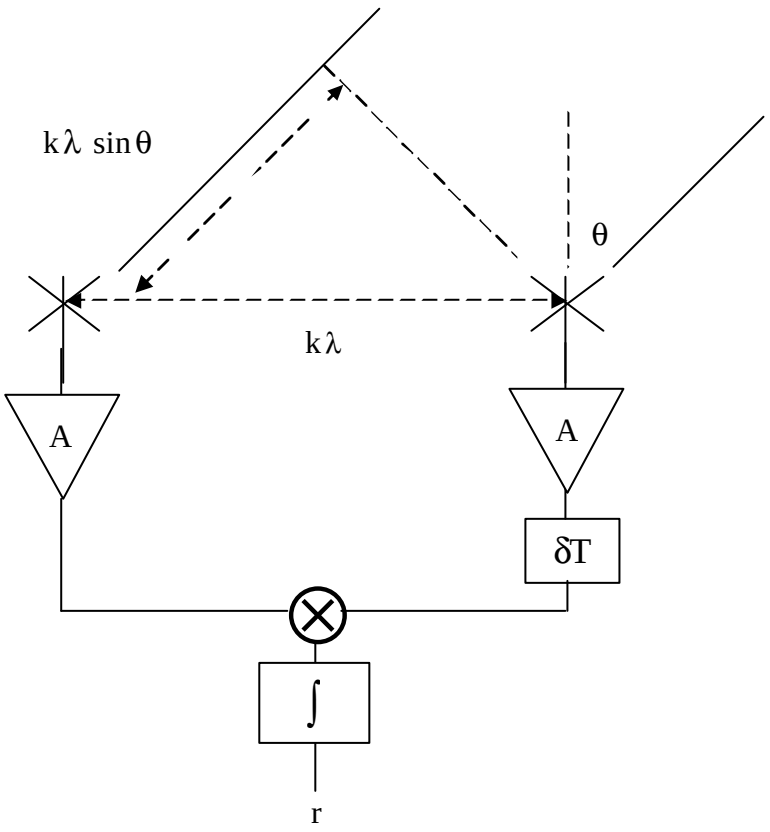


Figure 3.1 Two-Element Correlated Antenna Phased-Array.

Under ideal conditions, a point source in space presents to the antennae outputs the same electrical voltage, as a function of time. The spacing of the two antennas and arrival angle determine the time that the incoming wavefront needs to be delayed. The result r of the correlation function [3] is given by eq. (3-1):

$$r = \frac{1}{2T}\int_{-T}^{T} V(t)V(t-\tau)dt \qquad (3\text{-}1)$$

Similarly to the Fourier series analysis formula, the integrator has an integration time of 1 / 2 T. Therefore, the output from the multiplier is accumulated for 2T seconds and initialises to zero after the sum has been recorded. The output of the correlator represents power, as it is the voltage squared [3]. For the riometer, the bandwidth would be set to 1 MHz maximum. The ratio $1 / \Delta f$ equals 1 us. The integration time would be set to a typical value of 1 sec, which is much larger than $1 / \Delta f$. CN is considered as a continuous random process that results in a broad spectrum, of which the phases are a random function of frequency. The time-averaged CN amplitude in any finite band is constant with frequency over the passband of the receiver. In practical radio interferometers the input signals to the correlator may contain partially correlated signals from a partially resolved source, as well as, additional instrumental noise. These signals are processed using the cross-correlation function.

3.3 Cross-Correlation in Riometry

The cross-correlation function of two no identical signals, is given by eq. (3-2):

$$r(\tau) = V_1(t) * V_2(t) = \frac{1}{2T}\int_{-T}^{T} V_1(t)V^*_2(t-\tau)dt \qquad (3\text{-}2)$$

The integration time of 1 s is long compared to the reciprocal of system's bandwidth. In terms of digital signal processing extra hardware resources are required to implement the 1/2T function. For the dual-channel correlator versions in this chapter, the division is implemented in hardware. If any multi-channel versions are required, the division could be achieved in software at the host.

3.4 VHDL Modelling for the Complex Cross-Correlator

In terms of digital signal processing, equation (3-2) for the complex cross-correlation algorithm is rewritten in the discrete-time domain as:

$$\rho_{xy} = \frac{1}{N} \sum_{n=0}^{N-1} (x * y^*) \tag{3-3}$$

The appropriate phase delay is applied by using an analogue butler matrix or digitally by a beamformer. The integration time 1/2T is equivalent in the digital domain to the product of samples to be integrated, multiplied by the sampling period. Numerical techniques calculating the integration function, assisted in substituting the integration with the sum-of-products function [141].

Signal x and y represent complex number signals of the form:

$$x = a + j\,b \text{ (Cartesian)} \Rightarrow x = A(\cos a + j \sin a) \text{ (Polar)} \tag{3-4}$$

$$y = c + j\,d \text{ (Cartesian)} \Rightarrow y = A(\cos b + j \sin b) \text{ (Polar)} \tag{3-5}$$

The complex conjugate of y, as required by (3-3) equals:

$$y = r(\cos b - j \sin b) \text{ (Polar)} \tag{3-6}$$

The complex multiplication of $x * y^*$ equals:

$$r(\tau) = x * y^* = A^2\,[(\cos a + j \sin a)(\cos b - j \sin b)] =>$$

$$r(\tau) = A^2\,[(\cos a * \cos b + \sin a * \sin b) + j(\sin a * \cos b - \sin b \cos a)] \tag{3-7}$$

For the auto-correlation function of two identical signals, eq. (3-7) is rewritten as:

$$r(\tau) = A^2\,[(\cos^2 a + \sin^2 a) + j(\sin a * \cos a - \sin a \cos a)] = A^2 \tag{3-8}$$

In the digital domain all the products of A^2 by cos θ or sin θ of eq. (3-7) are represented by discrete binary values ranging from 0 to 2^n - 1, where n is the bit resolution. These values contain both the CN amplitude and phase [142]. Thus, eq. (3-7) takes the form:

$$r(\tau) = x^* y^* = (I_1 I_2 + Q_1 Q_2) + j\,(Q_1 I_2 - I_1 Q_2) \qquad (3\text{-}9)$$

where:

$$I_1 = A\cos a,\ Q_1 = A\sin a,\ I_2 = A\cos b,\ Q_2 = A\sin b$$

For a standard multiplication of complex numbers the results would have been:

$$r(\tau) = x^* y = (I_1 I_2 - Q_1 Q_2) + j\,(Q_1 I_2 + I_1 Q_2) \qquad (3\text{-}10)$$

In terms of hardware design the additional complement function of y is not adding any complexity. The adder and subtracter modules swap positions within the circuit. Based on eq. (3-10), the complex multiplier is built using four multipliers, an adder and a subtracter, as in the block diagram of Fig. A.1 in App. A.

For the test system, the I and Q resolution is set to 12-bits. The multiplier has two parallel 12-bit input data busses, a [11:0] and b [11:0]. Multiplication produces a 24-bit output. The $Q_1 I_2$ and $I_1 Q_2$ are added to produce the imaginary part of eq. (3-10). The sum of two 24-bit numbers is a 25-bit number. Two's complement arithmetic is used for the addition. The $I_1 I_2$ and $Q_1 Q_2$ products are subtracted to generate the real part of eq. (3-10). The subtraction of two 24-bit numbers is a 2's complements 25-bit number.

The 25-bit outputs of the complex multiplier are integrated and sent to the comparator, which controls the data flow. It outputs the result, when triggered by the controller. The results are passed to two 32-bit dividers. Each divider performs the 1 / N function on the I and Q channels, respectively. N is the number of samples integrated, according to eq. (3-3). The outputs of the dividers are buffered for 1 clock cycle for the I channel and 2 clock cycles for the Q channel. The extra delay on the Q channel allows better data management. As it is shown in a later section, the two channels are combined to one, making FIFO storage easier. The full complex cross-correlator is presented in the schematic of Fig. 3.2.

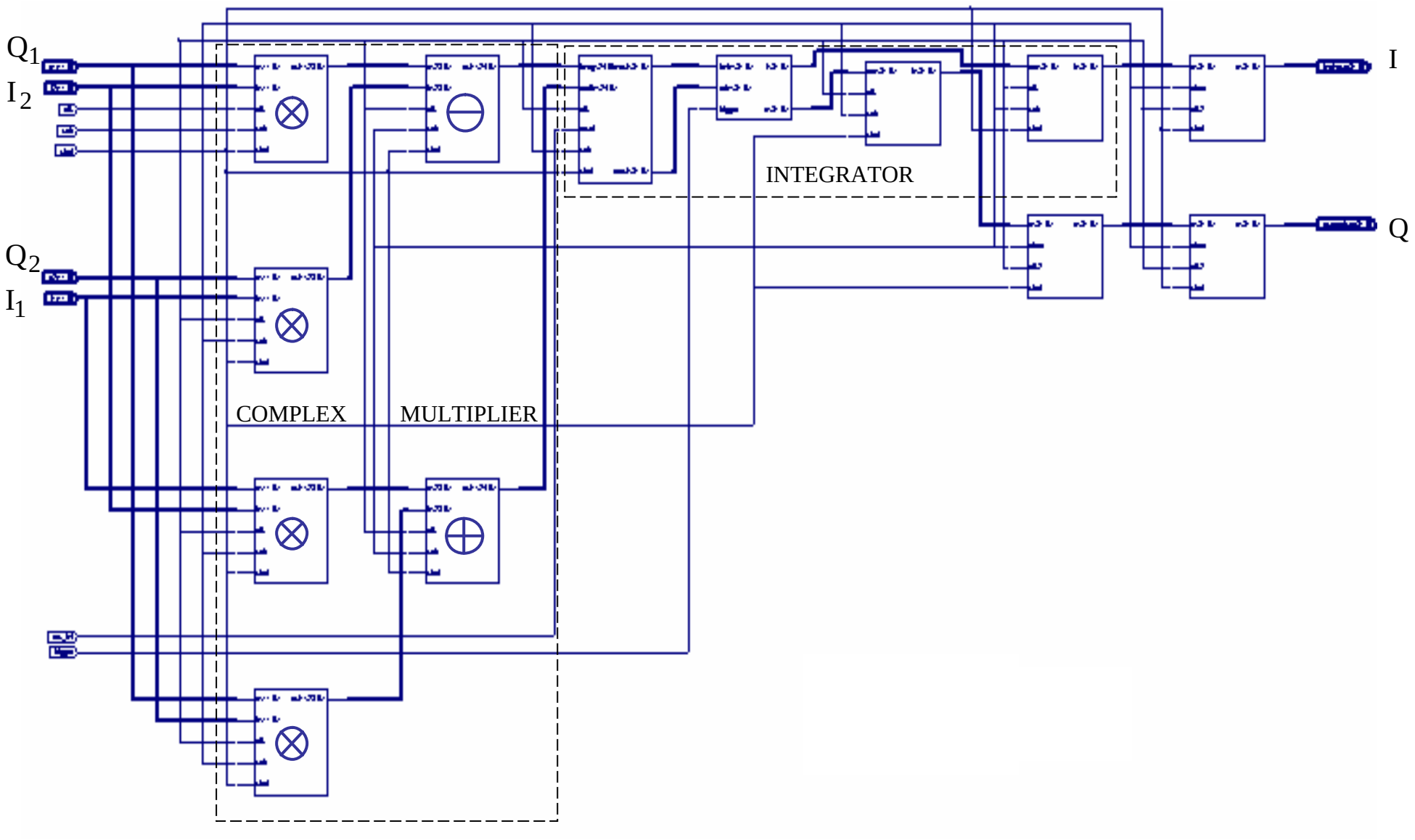


Figure 3.2 Complex Cross-Correlator's Block Diagram.

3.5 Functional Simulation Results for the Complex Cross-Correlator

The cross-correlator consists of several modules. It performs complex multiplication, integration and division by the number of integrated samples. The three actions are illustrated in Fig. A.2.

The signal buses z, tmp2, tmp3 and tmp4 hold the result of the I1xI2, Q1xQ2, Q1xI2, Q2xI1 multiplication products, respectively. Tmp5 [24:0] bus retains the addition result of the I1xI2 + Q1xQ2. The bus tmp6 [24:0] holds the outcome of the Q1xI2 – Q2xI1 function. Buses x7 [31:0] and y8 [31:0] contain the value as presented at integrator output. In this test, the integration time is set to zero. Accurate control of the integration module is achieved by the design of the master controller, explained in a subsequent section. The last crucial stage of the cross-correlator, based on eq. (3-5) is the division by the number of integrated samples. To verify the divider module, the division ratio is set to two. Buses tmp11 [31:0] and tmp12 [31:0] carry the division result.

3.6 VHDL Modelling for the Complex Waveform Generator

A complex waveform generator is required to provide the cross-correlator with an input. It is an inexpensive way to test the behaviour of the correlator to non-simulated data. Both modules coexist inside the FPGA. The unit has two sinusoidal outputs separated by 90° phase difference. They represent the in-phase and quadrature components of an arbitrary signal received from space. The complex sinusoidal generator is illustrated in Fig. A.3. The frequency of the output waveforms is set to be 1 MHz, the same as the bandwidth of the receiver.

The module consists of two independent address generators, a 32 x 12 ROM module and a buffer at the output. The address generator is designed as a five bit up counter. It is capable of scanning the full contents of the ROM in a sequential mode. External initialises the module to the desired phase. The ROM stores the values of a sinewave with 0 degrees phase sampled at 32 points using a resolution of 12 bits. Other techniques that provide the same output were also attempted. The design in [143] and uses the minimum amount memory and efficient waveform reconstruction at the output of the generator. It minimises the need for embedded memory hardware resources and uses the ROM differentially.

3.7 Functional Simulation Results for the Complex Waveform Generator

The functional simulation for the 12-bit complex sinewave generator is in Fig. A.4. The sin [11:0] and cos [11:0] carry the in-phase and quadrature values. The simulation runs at 32 MHz. This clock signal is the PCI bus frequency and connects directly to the FPGA. The period of a full cycle is given by eq. (3-11)

$$T = 32 * 31.2 \text{ ns} = 998.4 \text{ ns } (1.0016 \text{ MHz}) \qquad (3\text{-}11)$$

The rc1 [4:0] and rc2 [4:0] busses initialise the generator to the desired phase. The target waveform frequency of 1 MHz is verified.

3.8 VHDL Modelling for the Direct Digital Synthesiser and Controller

Using two DDSs generating the required I and Q sinusoidal waveforms for both channels produce similar results to Fig. A.4. The method later implements the digital down converter (DDC). The design of a DDS is presented in Fig. 3.3 [144].

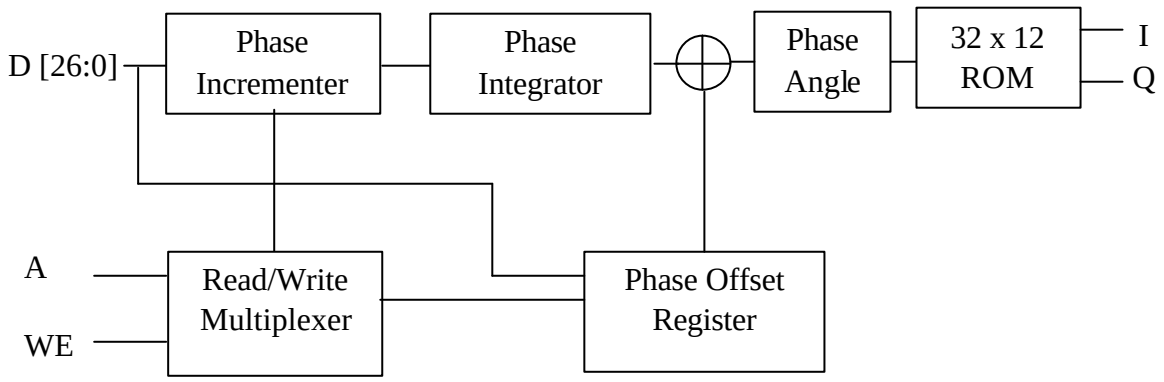


Figure 3.3 DDS Block Diagram.

In the previous section, the ROM holds 32 samples of the sinewave. The phase accumulator provides the required phase to retrieve each sample of the complex waveforms. The quantised phase angle module accepts the high-definition phase angle and decodes it to a lower resolution value, suitable for addressing the memory. The first DDS produces two fixed-frequency I and Q waveforms of 1 MHz. The circuit has -72 dB spur suppression.

The number of data input bits for the phase integrator is:

$$N_{acc} = \log_2 \left\lceil \frac{f_{operation}}{\Delta f} \right\rceil = \left\lceil \log_2 \frac{32*10^6}{0.25} \right\rceil = \lceil 26.9315 \rceil = 27 bits \quad (3\text{-}12)$$

The table depth N equals to:

$$N = 2^{12} = 4096 \text{ samples} \quad (3\text{-}13)$$

The phase-offset is:

$$\vartheta_{offset} = N \frac{\delta\vartheta}{360} = 0 \quad (3\text{-}14)$$

since no offset is required for the experiment. The phase increment is given by eq. (3-15):

$$\Delta\vartheta = \frac{f_I 2^{N}acc}{f_{operation}} = \frac{1MHz\, 2^{27}}{32MHz} = \frac{2^{27}}{32} = 4194304 \quad (3\text{-}15)$$

The phase increment value to program the phase accumulator is expressed in binary as:

$$\Delta J = 00001000000000000000000000$$

The DDS controller is a 7-states state machine. The A output switches between the phase increment register and phase offset register. When A = 0, D represents phase increment of 4194304. When A = 1, D carries the phase offset register value. The switching effect of A is effective when the WE (Write Enable) signal is 1. RDY is a handshaking output indicating that the DDS is programmed and ready to resume normal operation.

For the second channel of the 8-phase auto-switching DDS, a separate DDS controller was implemented. The second controller is modelled as a 55-states state machine. Therefore, the complex waveform generator of Fig. A.3 is chosen for the system, instead of its equivalent DDS circuit of Fig. 3.3.

3.9 Functional Simulation Results for the Digital Synthesiser and Controller

The functional simulation results for the DDS and controller for the I and Q waveforms, with a 0-phase offset, are in Fig. A.5. The frequency of the output waveform is 1.0016 MHz, similar to the result of the complex wave generator of section 3.7. The operation of the DDS and its controller for system's channel-1 is verified.

The results for the 2nd channel DDS and its 55-state controller are in Fig. A.6. The period is 998.4 ns (1.0016 MHz). The controller switches between the 8-phases every time the integration time is over. The 2nd channel DDS and controller are verified.

The comparison in terms of performance and circuitry complexity between the complex waveform generator and DDS yields to two conclusions: The DDS results in a greedier implementation in terms of hardware resources, while its functionality remains the same. The complex wave generator of section 3.6 is the optimum choice.

3.10 VHDL Modelling for the FIFO Module and Controller

This section describes the design of the FIFO module and control routing the correlator's output to memory and from memory to the PCI bus. The top-level block diagram is in Fig. A.7. The correlator's outputs in Fig. A.1 exit the unit in an I followed by Q mode.

The two-to-one multiplexer (mux2) in Fig. A.7 is responsible for writing the data to the RAM. Buses a [31:0] and b [31:0] are the I and Q inputs. Wi and Wq inputs are coming from the master controller analysed in section 3.11. They control the write action to the RAM for either I or Q inputs. They are synchronised with the arrival of I or Q in the sense that when there is an I value, Wi goes high and routes this value to the RAM. Similarly, when a Q value is active, Wq goes high. In this way, the even number addresses of the RAM are occupied by I values, while the odd number addresses by Q values.

The "level" module is a key component for the overall system. It outputs the current memory level in 9-bits and scans through the entire memory. It prevents accidental reading or writing to memory when the memory is empty or full, respectively.

The “write flags” module is taking into consideration the request for a read or write action and in conjunction to the “memory level” output asserts three types of flags regarding the write operation. These are the “write empty”, “write nearly full” and “write full”. When the memory level reaches the value 507 the “write nearly full” flag goes high. At the threshold of 511 the “write full” flag is asserted and no further writing is allowed on the memory. The next action is to read all the contents of the RAM before a new write cycle starts.

Two things must be specified, in order to write to the memory: measurement data and address. Since the multiplexer holds the data, the write address generator needs be designed. The write address generator is checking whether the s (write) input is high and the “write full” flag is low, before it increments the write address. When a value is written at the last memory location, the read input is activated and the PCI channel is enabled to carry the data. As soon as the read cycle starts, data is overwritten starting at location 0.

The “read flags” module supervises the read process. The module takes into consideration the status of the write or read input, the current position of the memory pointer and the “write full” flag before reaching to a decision. It has four output flags that inform the system regarding the progress of the read cycle.

The i_rf (read full) flag is asserted high when the write cycle is completed and the memory level pointer is at the last position. Permission is given to read the memory. In the read cycle, the i_r1e (read almost empty) flag goes high when the memory level reaches location 2. At the next cycle, the assertion of i_r1e activates the i_re (read empty) flag. The i_rne (read nearly empty) flag goes high when the memory pointer has incremented to location 5. The read cycle continues until the whole memory is read. Attached to the “read flags” module is the “read address generator”. It scans the memory contents.

The memory module used in this design is a synchronous dual-ported memory using BlockRAMs for Virtex II [145]. This is a true first-in-first-out (FIFO) design, since the first cross-correlated value to be written at location 0 coincides to be the first one to be read and output. The width is 512 words and depth of 32 bits. Its architecture allows concurrent write to two different locations and concurrent read from the same location.

The parallel input bus d [31:0] supplies the data to be written in memory. The parallel output bus q [31:0] provides the data to the PCI control circuit and from there to the PCI bus. The bus outputs a value from a certain memory location, stipulated by the read address generator, during the read cycle.

Busses da [8:0] and qa [8:0] indicate memory location to write or read a value, respectively. They are the output of the write and read address generators. The w input is the write enable of the RAM. It connects to the WEA input. The r input is connected to the ENB signal of the RAM. It authorises memory access using the read mode to the port B.

The FIFO works in two different frequency domains. In this design CLKA and CLKB are using the same frequency.

3.11 Functional Simulation Results for the FIFO Module and Controller

Based on the complexity of the design, the results are split into two sections. A set of results are presented firstly for the write cycle and, then, for the read cycle. The major input and output signals from the previous sections are present. The FIFO and controller modules are appropriately connected to the cross-correlator.

The I and Q busses are the integrated in-phase and quadrature values from the cross-correlator. Both busses stay to 0 during the time that cross-correlation takes place. As soon as the integration time is completed, two I and Q values exit the unit. The multiplexer is triggered by the w_i_t (write I) and w_q_t (write Q) signals and places these values sequentially on the output bus d [31:0].

The w_ram (write to ram) signal, which synchronises with the appearance of I and Q is activated and causes the write address generator to increment its value from 0 to 1, via the da [8:0] bus. The first two cross-correlated values 4194364 and 0 are written to memory locations 0 and 1. The memory level module is triggered by the write process and increments the memory location pointer from 0 to 1, meaning that the first two locations are occupied. Simultaneously, the i_we (write empty) and i_re (read empty) flags are switched to low. The system being in the write mode performs the above procedure until memory location 511, as in Fig. A.9.

As expected, both the i_wf (write full) and i_rf (read full) flag switch to high, as soon as memory location 511 is filled. The system is alerted in advance about the possibility of the memory being filled up, due to the i_wnf (write not full) flag. The flag is asserted when the memory pointer reaches location 507. The read cycle is ready to start.

Immediately after permission is granted to transmit data through the PCI bus, the r (read) signal is asserted high for the next 511 clock cycles, as in Fig. A.10. This does not prohibit the next write process to write data to the memory. It is going to write into locations that have already been read and sent to the PC. At 32 MHz the read process lasts for:

$$Dt\ (\text{read cycle}) = 512\ \text{memory locations} * 31.2\ \text{ns} = 15.9755\ \text{us} \qquad (3\text{-}16)$$

In a typical cross-correlator system, with integration period of 1 sec, all 511 memory locations are read, long before even the first I and Q values of the next write cycle arrive. Even if the memory has to be increased, as in the case of a multi-channel riometer system, the read time would still be far smaller than the integration time.

The q [31:0] sequentially outputs the values stored in the memory starting from location 0, with reference to the read address bus qa [8:0]. The memory level pointer decrements in steps of one every time a location is being read. As expected, the read and write flags go to 0 at the start of the read cycle, while the “write nearly full” at location 507. The end of the read cycle is illustrated in Fig. A.11.

The address generator has authorised access to all 512 - memory locations. The memory level pointer resets. The i_rne (read nearly empty) flag asserts high at location 508. The i_we (write empty) and i_re (read empty) flags rise at the last location. The system waits until the memory is filled up for a second time to initiate the next read cycle.

The operation of the FIFO module and FIFO controller is verified.

3.12 VHDL Modelling for the Frequency and Phase Controller

The controller is designed as a 17-states state machine and its connections are in Fig. A.12. The controller supervises and programmes the I and Q waveform generator, cross-correlator, FIFO and FIFO controller, as shown in Fig. A.13.

The input clock frequency is the 32 MHz PCI bus clock. The reset is connected to the reset output from the PCI bus. The arc1 [4:0] and arc2 [4:0] busses control the phase of the I and Q waveforms of the riometer channel one, respectively. In this experiment, channel one is set to a fixed phase of 0 (00000 binary) and 90 (01000 binary) degrees for I and Q, respectively. The rc1 [4:0] and rc2 [4:0] busses control the phase of the I and Q waveforms of channel two, respectively. They are initialised at 0 and 90 degrees. The first integrated values represent the auto-correlation function. As soon as the integration time overlaps, the controller switches the phase of the channel two by 45 degrees. The difference between the I and Q outputs of the generator maintain the initial 90 degrees phase difference. The new relation is 45 / 135 degrees.

Angle (degrees)	**Rc1 [4:0] (binary)**
0	00000
45	00100
90	01000
135	01100
180	10000
225	10100
270	11000
315	11100

Table 3-1. Phase Angle and Digital Value Relationship.

The controller provides the switching to all possible 8 phases (8 x 45 = 360 degrees) and eventually returns to the auto-correlation function. Table 3-1 shows the relationship between phase and the required rc1 [4:0] values.

The SCLR output resets the I and Q generator every 32 samples. The start signal is the CE (clock enable) input to the I and Q generator, the FIFO and the FIFO controller. The start2 signal is the CE input of the cross-correlator. Start2 is activated during normal operation. The integration time is controlled by the controller with tr and cn [4:0] signals. Whenever cn reaches 31, tr asserts high. Every time the integration time overlaps, the integrator is triggered by the trigger signal, to output its current value. The integrated value is stored and the cross-correlator is reset by the res_int (reset integrator) signal. Each of the I and Q integrated values is accompanied by the appropriate "write to FIFO" signal. The w_i and w_q signals trigger the FIFO multiplexer to queue the I and Q values to one channel. The w_ram (write to RAM) signal authorises writing of the integrated values to the memory.

3.13 Functional Simulation Results for the Frequency and Phase Controller

The results for the controller are in Fig. A.14. The CLK frequency is 32 MHz (T = 31.2 ns). The arc1 [4:0], arc2 [4:0], rc1 [4:0] and rc2 [4:0] phase control busses cycle through the values of Table 3-1. Every 8.4864 us the system resumes the auto-correlation function. The period of each switching phase equals to 1.0608 us for 34 cycles.

3.14 VHDL Modelling for the 8-Phase Dual-Channel Cross-Correlator System

The 8-phase auto-switching dual-channel riometer is in Fig. 3.4. The DDSs are initialised to autocorrelation. The system remains at this state, until the integration time overlaps. The DDSs and integrator are reset. The second DDS obtains the new offset phasing of 45 degrees. The cross-correlation is tested for an integration time equal to the period of the I waveform. The reset procedure is repeated indefinitely. At each switching cycle the two channels have an offset phase between 0 and 315 degrees, with 45 degrees step.

When the FIFO pointer reaches 507, the PCI interface requests permission to initiate a DMA transfer. Permission is granted and the results are temporarily stored to an application buffer at the host. The application buffer has size up to 8 MB. The DMA uses bursting, which holds the PCI bus engaged until all data are retrieved from the memory and saved to the buffer. The data bus tristates to the idle state. When the buffer is filled its contents are fetched by the C program and saved to a text file with a unique name. The text file is plotted using Matlab. The master controller supervises the operations synchronously.

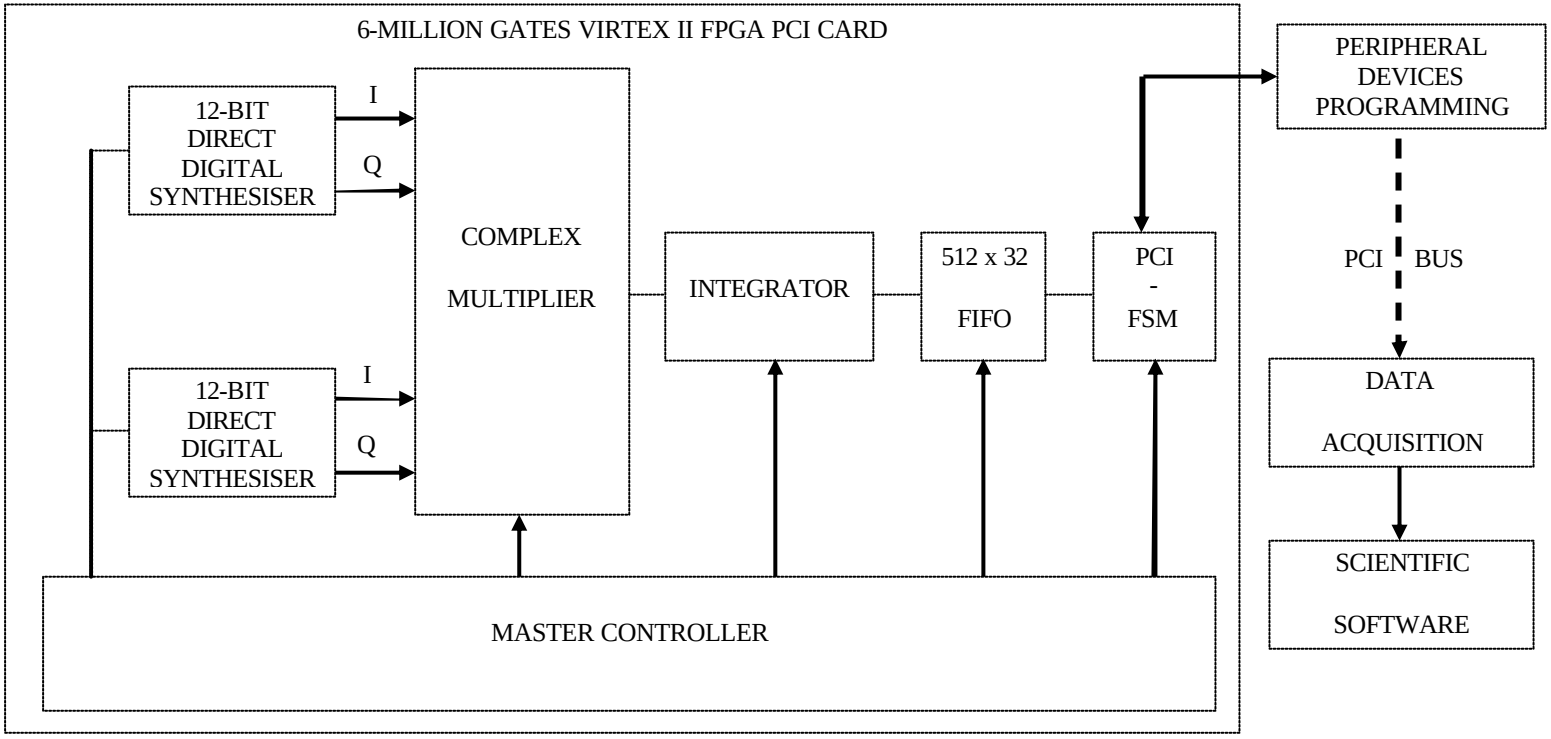


Figure 3.4 8-Phase Dual-Channel Cross-Correlator System.

3.15 Functional Simulation Results for the 8-Phase Dual-Channel Correlator System

The results of the 8-phase auto-switching dual-channel correlator system are in Fig. 3.5. The cross-correlated values, as presented to the FIFO, are represented by the I [31:0] and Q [31:0] busses.

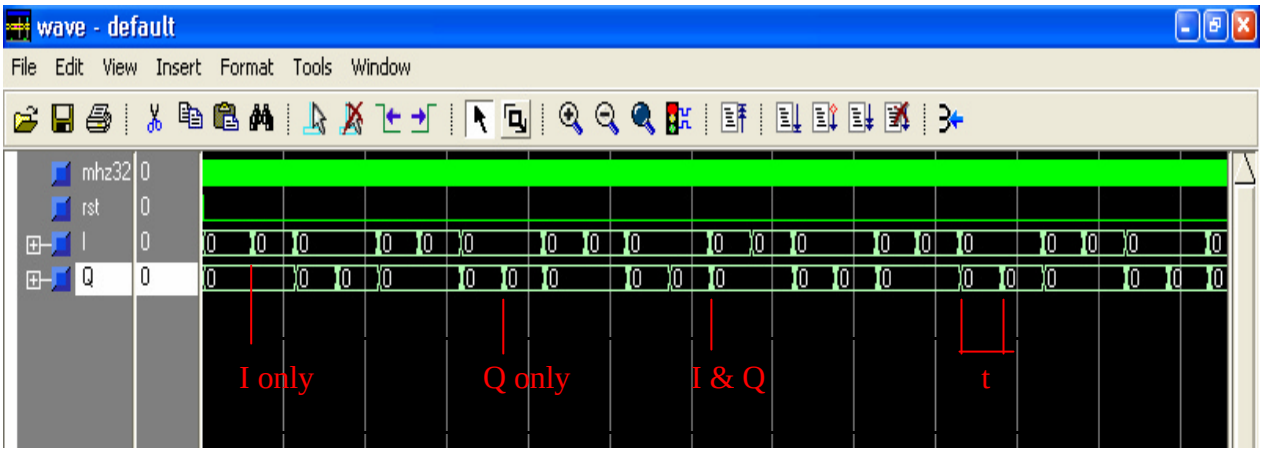


Figure 3.5 Cross-Correlator Results for the 8-Phase Auto-Switching Dual-Channel System.

Fig. 3.5 shows the results' periodicity, arising from the phase difference between the input signals. The cross-correlated results integrated over one full I period, are in Table 3-2.

0 / 90 x	IN PHASE	QUADRATURE	VECTOR (Polar)
0 / 90	4194365	0	$4194365\angle 0^\circ$
45 / 135	2965864	2965864	$4194365\angle 45^\circ$
90 / 180	0	4194365	$4194365\angle 90^\circ$
135 / 225	-2965864	2965864	$4194365\angle 135^\circ$
180 / 270	-4194365	0	$4194365\angle 180^\circ$
225 / 315	-2965864	-2965864	$4194365\angle -135^\circ$
270 / 0	0	-4194365	$4194365\angle -90^\circ$
315 / 45	2965864	-2965864	$4194365\angle -45^\circ$

Table 3-2. Cross-Correlation Results Integrated Over 1 Cycle.

For phase offset between the two channels of 0 or 180 deg., the result is a vector with large real part and zero imaginary. The positive and negative sign means the signals are in-phase or out-of-phase, respectively. The vector has amplitude of 4194365 and rotates 45 deg. anti-clockwise every t. For instance the $4194365\angle -135^\circ$ polar vector equals to $-2965864 - j2965864$ in Cartesian coordinates.

For phase offset of 90 or 270 deg., the vector lies on the imaginary axis of Fig. 3.6. The signals are orthogonal. The positive and negative sign of the value means that channel two leads by 90 deg. or lags by 90 deg., respectively. Similar analysis applies for all positions.

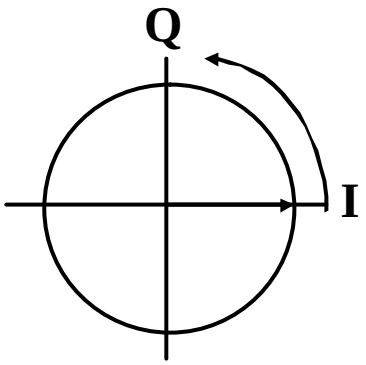


Figure 3.6 Cross-Correlation Results Presented as a Rotating Vector.

Another important feature about the results is that the constant vector amplitude is the square of amplitude A, as given by eq. (3-17).

$$\sqrt{A} = \sqrt{4194365} = 2048 \qquad (3\text{-}17)$$

The result of eq. (3-17) is additionally verified by considering the case of the I sinusoidal waveform at the output of the DDS with 0 deg. phase offset. The first quarter of the wave takes values between 0 and 7FF hex (2047), resulting in amplitude of 2048. The results for the overall design, as seen by the PCI bus, are in Fig. A.15.

Fig. A.15 also verifies the results of section 3.1.3. The signals of the PCI interface are explicitly shown. LD [31:0] is the PCI data bus. It stays idle until the FIFO is nearly full and, when authorised, transfers its whole contents to the application buffer.

3.16 VHDL Modelling for the Dual-Channel Correlator System

The building blocks of the free-input dual-channel cross-correlator system are in Fig. 3.7. The two DDS I and Q channels are removed and the master controller functionality has been minimised, since all the logic that was previously providing the 8-phase switching capability is removed.

In terms of frequency management, the circuit is separated into two frequency domains. The master controller, the cross-correlator, the write side of the FIFO (Port A) and the write side of the FIFO controller operate with an external clock. The clock is derived from an ADC board and it is the same as the sampling frequency. Since the bandwidth is up to 1 MHz, two analogue-to-digital converters need to sample at 2 MHz, to comply with the Nyquist theorem.

The rest of the circuit operates on the PCI bus frequency. This includes the PCI interface, PCI controller, FIFO read Port B and read side of the FIFO controller.

Special design attention was required by the Memory Level module, with the Size [8:0] output. The memory location pointer is incrementing on a write cycle and decrements on a read cycle. A dual clock counter, with dual clock registers, is required similar to [146].

However, a straightforward dual clock register implementation still does not exist for Xilinx FPGAs. The solution depends on using the BUFGMUX_1 component, which acts as clock buffer with two clock signals multiplexing capability. The r (read) input is the multiplex select signal. When r = 0 (write cycle) the external clock is selected for incrementing the pointer. When r = 1 (read cycle) the 32 MHz is selected for decreasing the pointer. This solves the problem and allows the system to operate correctly.

The integration time is set to 0.5 sec. The t is achieved by integrating 0.5 * 2 M samples = 1 million samples at 2 MHz.

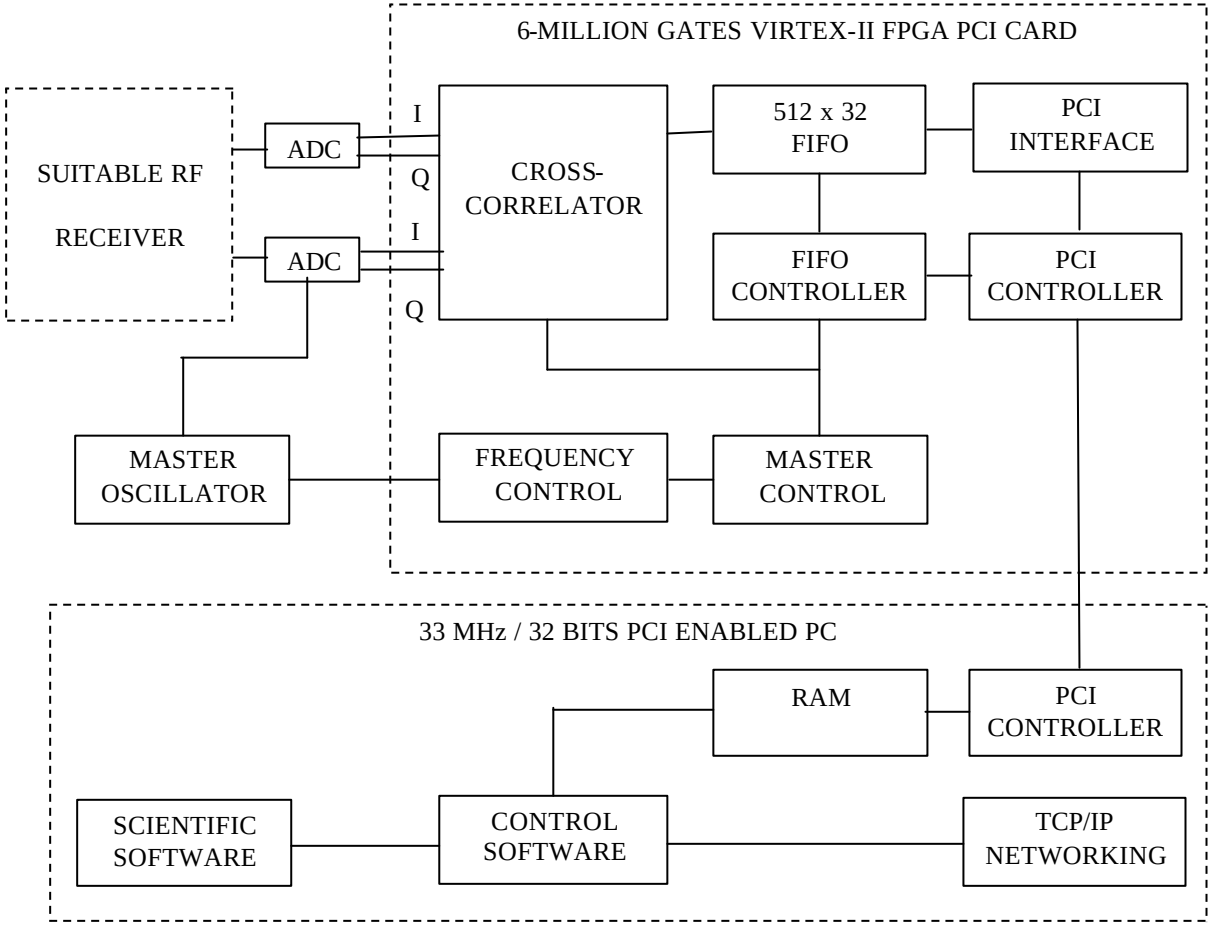


Figure 3.7 Free-Input Dual-Channel Cross-Correlator System.

3.17 Functional Simulation Results for the Dual-Channel Correlator System

The results for the dual-channel cross-correlator system are in Fig. A.16. The ld [31:0] bus initially loads the number of values to be transferred at each read cycle. This value is loaded to the ocount [29:0] bus. The bus stays idle for most of the time. As soon as the FIFO is nearly full, the request signal is asserted to transfer data on the PCI bus.

The actual transfer is triggered by the active low ldack_l signal. Two cycles after, the xfer1 signal triggers the fifo_read signal, which is the read input to the FIFO. It stays active until the transfer is completed. Similarly, the ld_oe enables the 32-bit output of the FIFO to be connected straight onto the PCI bus. The read process lasts 512 cycles and the ocount and FIFO level busses return to 0. The transfer is stopped by deasserting the lblast_l signal.

3.18 Hardware Implementation Results for the 8-Phase Dual-Channel Correlator System

The 2V6000-FF1152-05 Virtex-II FPGA has been targeted throughout the chapter. The FPGA is optimised for silicon area and high computational effort. The implementation process produces the required timing and configuration data. The implementation template controls how the software maps, places, routes and optimises the FPGA.

The MAP report (.mrp) contains warning and error messages detailing logic optimisation and problems in mapping logic to physical resources. The design summary is in Fig. A.17. The 36 warnings are due to the fact that although signals are declared in the top-level design, they are not used internally. For example, from the la [31:2] bus only signals la (23) and la (2) are used throughout the design. Therefore, the warnings are ignored.

The place and route (PAR) program takes an NCD file, places and routes the design and produces an NCD file, which is used by the bitstream generator (BitGen). PAR places and routes the design using a combination of the cost-based and timing-driven methods. In cost-based terms the placement and routing are performed using various cost tables, which assign weighted values to relevant factors such as constraints, length of connection and available routing resources. Using the time-driven method, the PAR places and routes the design based upon the timing constraints.

The number of signals not completely routed for a completely implemented design is zero, as for the 8-phase correlator. If it were not zero, the results are improved by using re-entrant routing or the multi-pass place and route flow. The results from the post layout timing report are in Fig. A.17.

After the design is completely routed, the device is configured to execute the desired function. Xilinx's bitstream generation program, BitGen, takes a fully routed NCD file as its input and produces a configuration bitstream. A bitstream is a binary file with a .bit extension.

The BIT file contains all of the configuration information from the NCD file defining the internal logic and interconnections of the FPGA, plus device-specific information from other files associated with the target device. The binary data in the BIT file is then downloaded into the FPGA's memory cells.

3.19 Timing Simulation for the 8-Phase Dual-Channel Correlator System

The timing simulation results for the 8-phase auto-switching dual-channel correlator are in Fig. A.18. The design operates up to a maximum frequency of 92 MHz. It is expected to be higher than the dual-channel correlator, since one clock source drives all the required logic, thus, the optimisation process would yield to more efficient results. However, more hardware resources are required, due to the size of the master controller and two DDS circuits. Detailed analysis of the timing results, checking internal register transfers and probing additional signals verify for a second time the operation of the 8-phase auto-switching dual-channel correlator system.

3.20 Hardware Implementation Results for the Dual-Channel Correlator System

The 2V6000-FF1152-05 FPGA is optimised for silicon area and high computational effort. The translation process results yielded to 0 errors and 0 warnings. The design summary is in Fig. A.19. The number of warnings is again 36. The reason is that top-level signals are declared but not used internally. These warnings are ignored as they do not affect the implementation results. The number of signals not completely routed is zero.

3.21 Timing Simulation for the Dual-Channel Correlator System

The timing simulation results for the dual-channel correlator system are in Fig. A.20. For simulation purposes, the circuit has two input clock signals the 32 MHz and 16 MHz. The active low reset signal is low for one cycle and stays high throughout the rest of the simulation. The active low request signal is activated, as soon as the FIFO pointer reaches location 507. For simulation purposes, the acknowledgment request signal is set to high since on the practical system its behaviour may vary a few cycles based on the host and PCI configuration.

The system performs periodical data transfers using demand-mode DMA with bursting. The burst signal guarantees that the whole contents of the memory would be sequentially read and that the transfer cycle would last exactly 512, not less. It is active high and asserted when the memory pointer reaches position 507.

The ld data bus initially programs the number of data values to be transferred. The value is stored to the ocount [29:0] bus. The PCI address bus la [23:0], the internal write2 and xfer2 signals and the lbe_l [3:0] bus determine the writing to the ocount [23:0] bus. The write2 and xfer2 signal are the output of the slave transfer state machine. The request signal is asserted and acknowledgement is expected. When the active low ldack_l signal is 0, it triggers the DMA state machine on channel 1 to activate xfer1 signal, which in turn activates the required fifo_read.

The PCI data bus stays idle until the FIFO is filled. The active high transfer signal supports the transfer and stays high during the data transfer time. During the read cycle the bi-directional 32-bit bus ld [31:0], possesses the current value retrieved from the memory. Each value is routed through the PLX 9656 controller's channel 1 to the application buffer.

The sampling frequency is 16 MHz yielding to a period of 62.5 ns. For this simulation 128 I and Q samples are integrated bringing the integration time to 8 us. The maximum frequency of operation is 80.67 MHz. The rest of the internal building blocks, such as the cross-correlator, master controller, FIFO and FIFO controller operate correctly. The discussion about the operation of these modules remains the same.

3.22 Experimental Results for the 8-Phase Dual-Channel Correlator System

The bitstream file is downloaded to the FPGA and data logging is initiated. A timer was added to introduce a delay of 10 min between each phase transition. The test lasts for 90 min for a full set of results. The integration time is 1 s.

The data logging process stores the received values into text files. A Matlab program was written to open these files and visualise the results. Each file contains 16384 (2^{14}) values. The 1st and 9th set-up, test the auto-correlation function. The results are plotted in Fig. 3.8 for a test duration of 90 min.

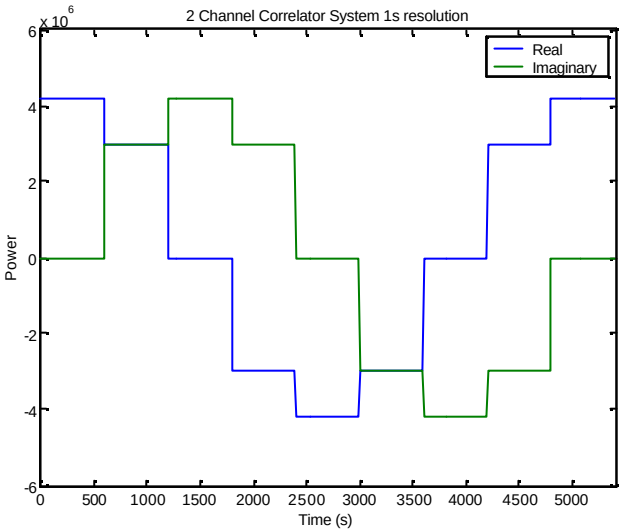


Figure 3.8 Test Results for the 8-Phase Dual-Channel Correlator System.

The results verify Table 3-2, showing the relationship between the numerical values, magnitude and phase of the corresponding vector. Additionally, the results match the functional and timing simulations, and overall verify the operation of the correlator system.

3.23 Conclusion

The 8-phase dual-channel and free-input cross-correlator systems have been successfully designed in VHDL, hardware implemented and downloaded to the Virtex-II 2V6000 FPGA ADM XRC-II board, which is connected to the ADC-PMC carrier board. The functional and timing simulation results, as well as, the downloaded design proved the correct operation and one-to-one correspondence with the mathematical models developed earlier in the chapter. Data logging has been achieved, in order to check the internal FPGA design, PCI interface design and data logging using C/C++ software.

The understanding of a two-element antenna array riometer assisted in developing the mathematical models to be implemented in VHDL. The autocorrelation function is used for identical signals. For any radio astronomy system, the correlator's input signals contain partially correlated signals and sidelobe interference, as well as, additional instrumental noise. These signals are processed in the digital domain by circuits such as the cross-correlator described in this chapter.

Both the amplitude and phase information of the incoming signals are processed by the correlator. The time domain complex cross-correlator consists of a complex multiplier and an integrator. The complex multiplier calculates the product of the input on channel 1 with the complex conjugate of channel 2. Practically it consists of four 12 bits multipliers, an adder and a subtracter.

The result is sent to the integrator that accumulates results until the integration time is over. Then, it outputs the result and it resets to zero. The results are properly stored to a FIFO, until the FIFO is filled. When it is nearly full the system asks for permission to transfer the data through the PCI bus to the custom size application buffer on the host PC. The data transfer is achieved using demand-mode DMA.

The 8-phase dual-channel correlator was built on these principles. It features a sophisticated way of switching between the offset phases between the two channels, a reliable FIFO controller and a complete PCI interface and control logic. The mathematical relation of the results was presented. The integrated I and Q values form a vector of constant amplitude and varying angle of 45 degrees steps. The amplitude is the square of

the I or Q waveform. The phase angle of the vector is the same as the phase offset between the two channels. The result analysis for the dual-channel cross-correlator system remains the same. It presents a simplified structure, compared to the phase switching version, and is capable of receiving external inputs on the two I and Q channels.

In terms of silicon usage the circuit proposed does not impose the implementation phase to strict design rules. The hardware requirements would change if a multi-channel version is desired in the future. The FIFO could be implemented by using the external ZBT memory. The divider could also be excused from the FPGA and implemented in software. A significant bottleneck for the design could be the size of the integrator. The larger the integration time the more powerful the integrator should be. In order to achieve an integration time of 0.5 sec, 1 million samples are integrated at 2 MHz. The integrated undivided I value is 4,398,110,474,240 (4.4 Trillions), represented by 43 bits and exceeding the 32 bits PCI bus. Two PCI clock cycles are required to transfer one result. A standard 64-bit HI & LO big-endian accumulator register architecture may need to be implemented in the future.

The 8-phase dual-channel correlator requires 550 out of 33,792 slices, which is roughly 1% of the chip. The VHDL coding yielded to an efficient implementation as there are no-unrelated logic circuits. 728 slice flip-flops and 695 4-input LUTs were used. One Block RAM implements the dual-port FIFO module. One GCLK clock buffer was used for the global 32 MHz clock signal. The correlator system requires a total of 95,315 gates, out of which 92,867 are equivalent 2-input NAND logical gates and 2,448 gates for the IOBs JTAG implementation.

The free-input correlator design occupies 443 out of 33,792 slices, which is approximately 1% of the chip. 662 flip-flop slices and 495 4-input LUTs were used, which is less than 1% of the available 67,584, respectively. One block RAM was used out the 144 and 4 multiplier blocks. It corresponds to less than 1% of the available resources. Overall, the design occupies 95,475 gates. 90,723 gates are used for the actual logic design and it signifies a reduction of 2,144 gates. 4752 gates are used for the IOBs JTAG implementation, which is an increase of 2,304. This is due to the significant increase of the correlator's I/Os.

One solution that would minimise the complexity of a multi-channel correlator version would be to use a 64 bits / 66 MHz PCI enabled PC. The performance of the system would be enhanced significantly. Only one data cycle would be required for each data transfer. Additionally, the retrieval and DMA transfer of the integrated values would take place at double the speed rate of which currently occurs, leaving a significant slack for other system operations.

A simplified version of the cross-correlator system is used in the following chapters describing the design of the Priamos widebeam riometer and Dimagoras magnetometer.

Chapter 4.

Novel Programmable Riometer for in-depth Ionospheric And Magnetospheric ObservationS (PRIAMOS) Using Direct Sampling DSP Techniques:

RF Receiver & Peripheral Hardware Design

4.1 Introduction

The following chapter describes the design of the Priamos RF Receiver unit and peripheral hardware. The programmable RF receiver allows multi-frequency and multi-bandwidth operation. The chosen architecture samples CN directly after the amplification stages. The receiver can be installed close to the antenna for minimum transmission line losses.

The receiver removes the noise balancing technique, extensively used in the past. Existing analogue riometers are processing 50% of the time the incoming signal and 50% the internal noise source. The technique is followed by a 3 dB loss of power. The RF receiver is continuously processing the input signal and exhibits improved performance of 3 dB, in terms of power levels.

Comparing to multi-stage receivers, any intermediate frequency (IF) mixer stages are eliminated and the receiver exhibits additional improvement of 6 dB. IF conversion stages apart from the desired sideband, introduce thermal noise, undesired sidebands and local oscillator (LO) leakage through the modulator to the IF signal. Using IF processing and depending on the RF background, the receiver may be dominated by thermal noise or background thermal-equivalent noise or interference may dominate the noise power. The single-step digital baseband translation restricts these factors to a minimum. The power dissipation of the different components and interference with the received signal is a crucial factor in selecting the appropriate components, since the received power levels are low.

4.2 Background

As in section 2.2.1, most widebeam riometers installed globally are built by La Jolla Sciences [147]. The La Jolla riometer uses the noise balancing technique, in Fig. 4.1.

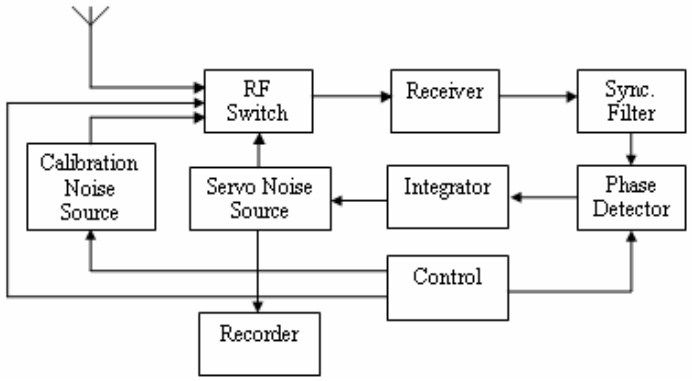


Figure 4.1 The La Jolla Widebeam Riometer.

The self-balancing receiver's internal servo-controlled type-5722 noise diode matches the antenna's noise power. The riometer switches between the antenna and noise source at 340 Hz. The switching frequency is derived from a LO. The mismatching of the antenna and noise diode signals generates a 340 Hz squarewave. The squarewave is amplified and detected by the phase detector. The detector's output voltage is proportional to the mismatching and the polarity depends on the strongest signal. The output voltage adjusts the diode noise power to match the antenna noise power, so their difference is zero. The diode's noise power is proportional to its current and the antenna's noise power is measured on a linear scale by recording the diode current on a pen recorder.

The operating frequency was determined as a function of ionospheric absorption. 27.6 MHz at high-latitudes, where absorption is high. At low-latitudes, 18 and 20 MHz were used. Most recent riometers built are at 30 MHz. The receiver is of dual-stage superheterodyne type. To avoid radiowave ionospheric interference, a swept-frequency and minimum-signal-detector scheme is implemented. The first-stage LO varies the frequency in 100 KHz steps every 40 s. The triangular frequency sweep is achieved by mechanically adjusting the capacitor determining the frequency of the first oscillator.

Reliable and stable over time receivers can eliminate the noise balancing technique. The Priamos system in Fig. 4.4, is simpler in concept, incorporating state-of-the-art features.

4.3 Receiver Design Study

There are three receiver architectures depending on the ADC position in the system. These are the baseband (BB), IF and RF. In 1994, the Watkins-Johnson company published its receivers' frequency plans [148]. The superheterodyne receiver [149] contains a filter, amplifier bank and two conversion stages. Each conversion stage has one LO, filtering and amplification. The conversion stage introduces thermal noise, unwanted frequency components and leakage of the reference signal into the wanted IF signal. Using one conversion stage, a 10.7 MHz IF signal is obtained, BPF to 250 KHz and sampled at 500 KHz, as in Fig. 4.2. This architecture has been used in passive wave radio experiments along with the noise balancing technique and it exhibits higher noise figure (NF), lower dynamic range (DR), there is no digital control over the analogue stages, low reliability factor, temperature drift and the calibration frequency is determined empirically.

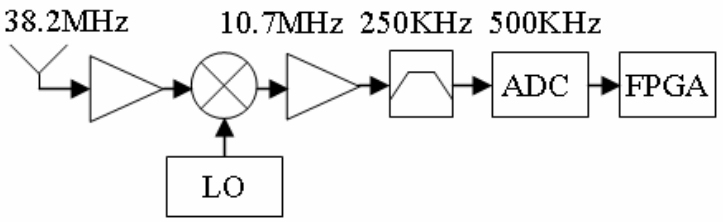


Figure 4.2 IF Receiver Architecture Solution.

Figure 4.3 RF Receiver Architecture Solution.

The ideal solution is the RF architecture of Fig. 4.3. CN is sampled at 2.5 times the centre frequency after the amplification and BPF stages. The high center frequency, sharp cut-off characteristics and low-stopband attenuation requirements impose a symmetrical FIR filter of 5000 coefficients. It requires 400 clock cycles to produce the first result, excessive hardware resources and yields to an expensive system.

By mutually excluding the other two techniques, the direct conversion [150] is chosen [151]. The RF signal is translated to DC in one step, as in Fig. 4.4. It can also translate to nonzero BB and demodulate the signal into BB bitstreams within the same circuit.

4.4 Priamos Specifications, Computer Architecture and Instrumentation

The Priamos system of Fig. 4.5, features the following:

- Multi-frequency (1 - 60 MHz).
- Multi-bandwidth (3 KHz – 1 MHz).
- Noise figure of 3.1 dB.
- 14-bits ADC resolution.
- 87 dB DR expandable to 175 dB. Saturation is avoided during Type III & IV SREs.
- Programmable integration time (1 ms – 22 min) for in-depth observation of events. Default is 1 s.
- 0 dB antenna transmission line losses.
- Reprogrammable GPS functionality.
- Auto-recovery from GPS loss of synchronisation.
- UTC referenced clock management and Real-Time Clock (RTC) support.
- Reconfigurable within milliseconds.
- Supports over 300 SDR commands for real-time programming and reconfiguration of the system.
- SRAM data storage up to 144 hours or real-time host transfers.
- Multi-port: RS232, USB 2.0 and 10/100 Mbps Fast Ethernet.
- Automatic calculation of QDCs and Absorption Values.
- Fast prototyping of other Space Physics Instrumentation projects.

Priamos consists of the RF Receiver Unit described in this chapter and DSP Engine Unit of the next chapter. An external programmable GPS receiver connects to DSP Engine via the grey RJ45 to DB9 female adapter in Fig. 4.5. The parallel black coaxial cable at the back of the instrumentation connects the GPS antenna to the GPS receiver.

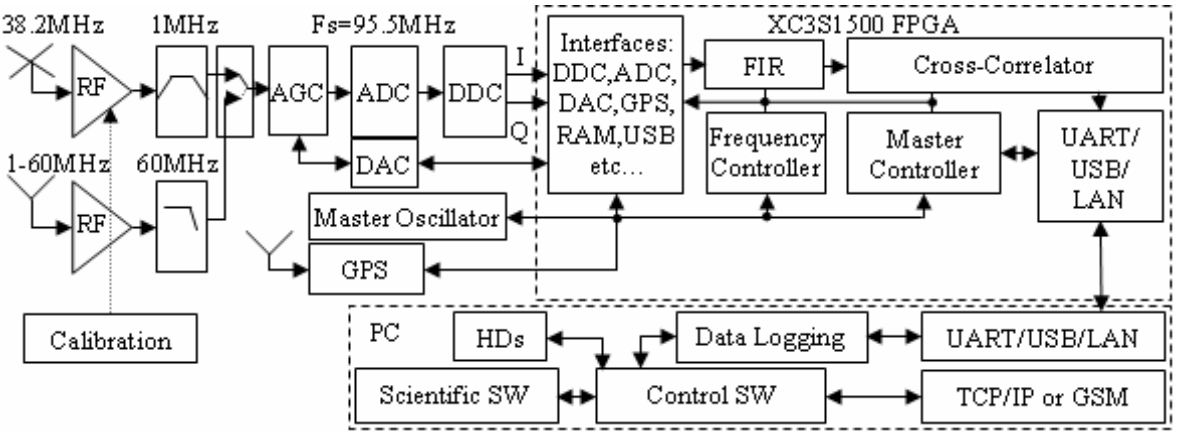


Figure 4.4 Priamos Computer Architecture.

Figure 4.5 Priamos Instrumentation.

The bi-directional communication between Priamos and host is via a 10/100 Mbps Fast Ethernet switch in Fig. 4.5. A dual power supply delivers the required 0V and 15V analogue, and 0V and 5V digital distribution voltages.

4.5 RF Receiver Design

The RF receiver board is split into five functional areas, namely RF input and calibration (RFIN/CALI), pre-amplifiers (PAs), RF filters, digital amplifier (DAC + AGC) and ADC circuits. The following subsections explain the operation of the different circuits. The top-level diagram of the Priamos RF receiver board is in Fig. 4.6. The RF receiver PCB consists of 140 components in ten A4 circuit schematic pages.

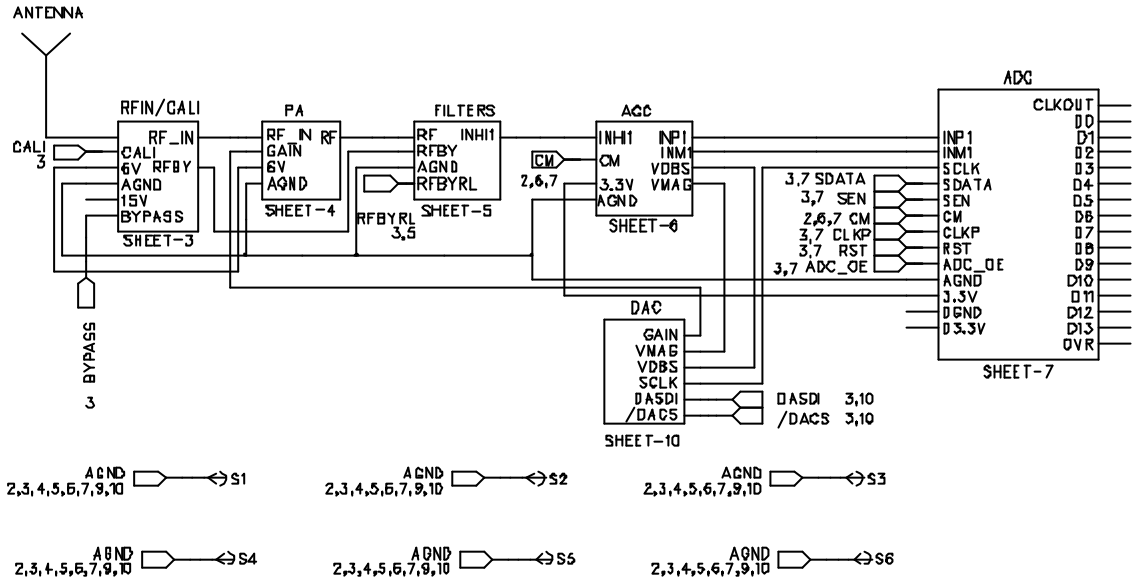


Figure 4.6 Priamos RF Receiver Board Top-Level Schematic.

The receiver connects to the crossed-dipole antenna, in App. B. The antenna was modelled using Mininec [152]. Mininec uses the Method of Moments (MoM) [153].

4.5.1 RF Input, Switching and Calibration Circuits Design

The RF input, switching and calibration circuits are in Fig. C.1. R1, D1 and C2 form a white Gaussian noise generator with flat frequency response over the 0.1 Hz – 100 MHz range. The noise generator is used for calibration. The Pi-network of R2, R3, R7, R8, R11 and R12 forms a 1 – 20 dB variable attenuator circuit. The attenuator defaults to 1 dB. Two RF relays of 0.02 dB insertion loss control the switching at the input of the receiver. The RF relays' digitally controlled circuit is in Fig. C.2. RL1 selects either the attenuator's output or the antenna input J1. RL2 demultiplexes the input signal to the 38.2 MHz BPF or 1 - 60 MHz LPF. By default, the antenna input is routed through the BPF.

4.5.2 Pre-Amplifiers Design

Two 50R impedance matched PAs are built based on the high performance, low-noise, silicon bipolar monolithic microwave integrated circuit (MMIC) MSA-0886 [154] of Fig. C.3. Both PAs have an adjustable gain of 32 dB and NF of 3.05 dB. The current through L6 is 32.7 mA. The first PA amplifies a 37.7 – 38.7 MHz signal, while the second a 1 – 60 MHz signal.

The 37.7 – 38.7 MHz amplifier has a loss of 0.2 dB due to the input and output capacitors and 0.1 dB due to the RF choke (L6) and bypass capacitor (C30). The total loss is 0.3 dB leaving a total gain of 31.7 dB. The 3rd order output intercept point (OIP) is 24.5 dBm. The 3rd order output intermodulation (IM3) level is -277.9 dBm. The group delay is approximately 300 ps. The 1 – 60 MHz PA has a loss of 0.22 dB due to the input and output capacitors and 0.09 dB due to the RF choke and bypass capacitor. The total loss is 0.31 dB leaving a total gain of 31.69 dB. The 3rd order OIP is 24.5 dBm. The 3rd order output IM level is -277.93 dBm. The group delay is approximately 300 ps.

Bipolar, FET, dual-gate MOSFET and BJT amplifiers in different configurations were also designed. However, the circuits' complexity (16 components for a BJT cascode amplifier), higher NFs (> 3.7 dB) and overall system performance concluded to the presented design.

4.5.3 Bandpass and Lowpass Filtering Design

Selectivity indicates the riometer's ability to select the desired signal and eliminate unwanted interferers, which could be stronger than the signal of interest. Similarly to gain, filtering performance is easier to achieve at low frequencies. A 1 MHz BPF implemented at centre frequency of 38.2 MHz requires a lower Q than a 1 MHz filter at 1 GHz. 250 KHz is 0.65 % of 38.2 MHz. At the frequency of interest filtering can be achieved using crystal or surface acoustic wave (SAW) filters [155-156]. Micronetworks produce SAW filters with centre frequencies between 50 and 1300 MHz, outside the range of interest. Microsonics produces military specifications BPFs between 10 MHz – 1500 MHz. The closest is the FB1071 at 42.384 MHz. The solution proposed is based on a custom made Butterworth BPF using image parameters. Coilcraft produces the less than 0.3 dB insertion

loss, 3rd order Butterworth S3LP606 LPF, with cut-off frequency of 60 MHz suitable for implementation into Priamos. The combined BPF and LPF solution is in Fig. C.4.

The 3rd order Butterworth BPF has BW of 1 MHz. The passband ripple is 0.4 dB. The circuit has minimum stopband attenuation of 80.572 dB at 28.734 MHz and 50.774 MHz. The input and output impedance is matched to 50 Ohms. Both inductance and capacitance spread is 2.913365 K. For the BPF datapath, BW is further reduced to the desired value by the FPGA. The RF relay (RL3) directs either the LPF or BPF path to the digital AGC circuit. The relay's digitally controlled circuit is in Fig. C.2.

4.5.4 Digital Amplifier Design

An adjustable gain differential amplifier levels the signal for the ADC to detect [157]. Amongst several manufacturers, AD produces several devices meeting Priamos requirements, such the AD603, AD8330, AD8369 and AD8370. The AD8330 [158] was chosen due to its flat BW up to 150 MHz, low-noise gain adjustment up to 50 dB and no phase inversion. The power supply is 3.3 V, compatible with the system. The resulting circuit is in Fig. C.5.

The differential input resistance of AD8330 is 1 KR. The RF relay's output impedance is 50 R. To achieve maximum RF power transfer and avoid transmission line reflections, the 50 R is matched to 1 KR. The parallel resistor R32 transforms 1 KR to 212 R, close to 200 R. A 0.02 dB insertion loss 1 - 4 RF transformer transforms the 50 R to 200 R.

The automatic gain controller (AGC) also converts the single ended output of the RF relay to differential. The peak differential input is +/- 2V. The voltage applied to Vmag determines the output voltage swing. It is set to 0.5 V for an output voltage of 2V. Gain control is applied by the voltage at Vdbs. Vdbs is set to a default value of 0.84 V for a loaded gain of 22 dB (28 dB unloaded). Vmag and Vdbs inputs are digitally controlled by the circuit of Fig. C.6. The combined circuits operation forms a digital analogue amplifier.

The AD5232BRU10 digital potentiometer (Digipot) [159] has been chosen. It offers 39R/position resolution, since it is a 10 K 256-position variable resistor. Priamos supports

all 16 instruction categories, issued to control the digipot, although 6 categories (10 instructions) are sufficient for real-time operation.

At reset, the digipot exhibits a gain of 22 dB. For 250 KHz BW and assuming data is routed through the LPF path, the total gain is 54 dB, OIP is 14.2 dBm, NF minimises to 3.05 dB, MDS is -117.02 dBm and 2 tone DR is 51.48 dB. The group delay is 2.7 ns, making the aggregate system's delay slightly less than 3 ns. The AD8330 exhibits a 3rd OIP of 14.2 dBm, which effectively becomes the system's OIP. The NF of the device is 4.2 dB, but it does not affect negatively the system's performance. For 100 KHz BW, MDS changes to -121 dBm and 2 tone DR is 54.13 dB.

The Mode input is unconnected, since reprogramming the gain direction is not required. The capacitor to the offset (Ofst) pin forms a 1 MHz HPF. Power-down and hibernation are not currently supported by Priamos. Since the AGC connects to the ADC of the next section, the external common-mode control input CNTR is used and set at 2.8 V.

The AGC and digipot circuits can be used for other Radio Astronomy projects, where similar digital amplifiers are required. If the antenna, PAs and BPFs are altered, the digital AGC circuits and the HW described in the following sections remain the same.

4.5.5 Analogue-to-Digital Converter Design

The choice of the ADC is based on the sampling frequency, number of bits, power dissipation, cost and availability of evaluation modules that would allow quick prototyping [160]. For compatibility purposes, AD and TI ADCs were examined.

During the device selection stage, TI released the 14-bit 125 MSPS ADS5500 (780 mW max, 70.5 dB SNR), while AD was offering the 14-bit 105 MSPS AD6645 (1.75 W max, 75 dB SNR) and the 16-bit 80 MSPS AD10678 (8 W max, 78 dB SNR). The sampling frequency must be at least 2.5 times the BPF centre frequency of 38.2 MHz (95.5 MHz), and the ADS5500 was chosen [161]. ADS5500 has one 14-bit parallel output (D0-13), over-range flag (OVR) and synchronous clock output (CLKOUT). The resulting circuit is in Fig. C.7.

The circuit is working at 95.5 MHz, driven by the FPGA controlled master oscillator of the next section. A digital PLL (DLL) is implemented inside the ADC for sampling rates over 80 MSPS. An FPGA controlled serial control register activates the DLL and programs the range of the sampling frequencies. When DLL is activated, the ADC operates in the 60 - 125 MSPS range. With DLL off the ADC operates in the 10 - 80 MSPS range.

If the FPGA is not programmed and no clock is present the ADC enters the power down mode. If the clock is between DC and 1 MHz or a serial command is sent to the chip, the ADC enters the power-down mode. In this mode the outputs tri-state and the DDC connected to the ADC awaits the re-initialisation process to resume operation. Only the internal reference is operating in this mode to shorten the waking time. The host PC issues the Power_Down_Off command for the ADC to resume operation.

Priamos ISA supports twelve instructions to control the ADC during real-time operation. These include programming of the DLL, normal operation, all outputs 0, all outputs 1, all outputs toggle, power down, ADC_OE and ADC_RST. The ADC is programmed via SPI. ADS5500's SPI timing diagram is different to AD5232's and a new hardware interface was implemented inside the FPGA.

4.6 Peripheral Hardware Design

The remaining major hardware peripherals to be interfaced by the Priamos DSP engine include the master oscillator and GPS receiver.

4.6.1 Master Oscillator Design

A single-chip master oscillator, implementing the PLL functionality [162] in a programmable manner, was required to drive the ADC, DDC and FPGA circuits. Based on the available products, Integrated Circuit Systems (ICS) provided the most interesting configuration. The ICS525-02 [163] produces an accurate, high-frequency clock signal up to 250 MHz. A simple crystal of any frequency between 5-27 MHz drives the chip. The output exhibits low jitter and duty cycle between 45 and 55, up to 200 MHz. The ICS525-02 and support circuitry is in Fig. C.8 (a). The power-up frequency is 25 MHz, controlled by the circuit in Fig. C.8 (b). For 95.5 MHz 0 ppm output a crystal of 10 MHz is used.

4.6.2 GPS Instrumentation

The system requires several synchronisation signals, such as:

- Programmable integration time, default 1 s. The cross-correlator releases the integrated result to memory or host PC.
- UTC time for in-situ data time-stamping. Each integrated value is time-stamped as soon as the cross-correlation is complete.

The host could supply the synchronisation signals if connected to a timeserver. For riometers with no internet access, the solution is to use a GPS receiver. A wide selection of GPS products exists [164]. The implemented GPS instrumentation is in Fig. 4.7.

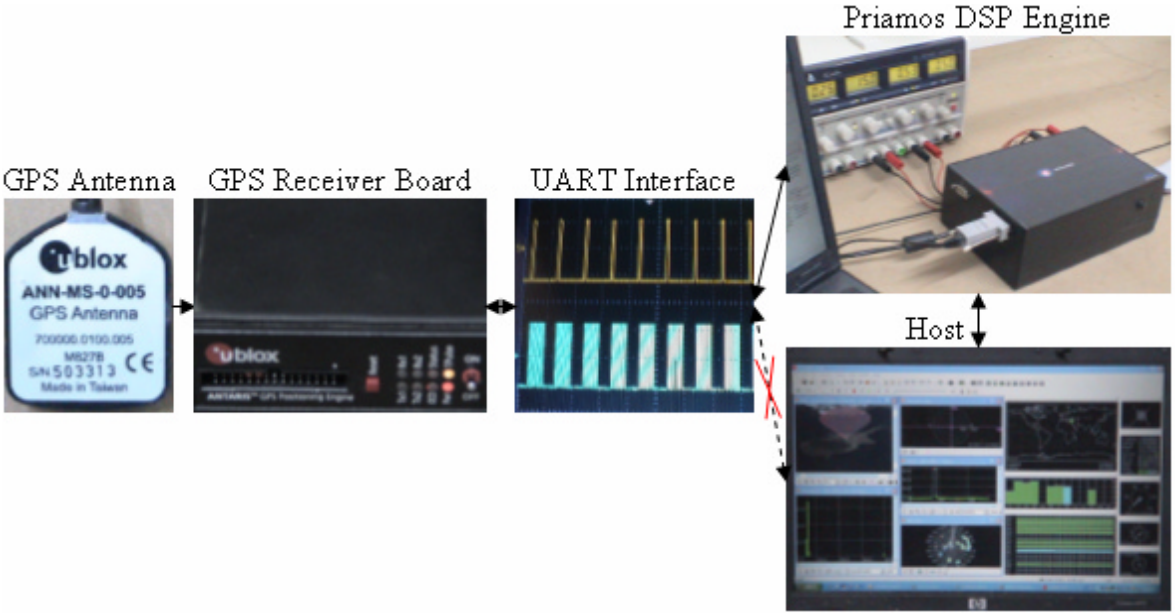


Figure 4.7 Priamos GPS Instrumentation.

The Antaris GPS Evaluation Kit [165] was used during prototyping mainly due to its reprogrammable functions. The receiver input is a MCX connector connecting to an active antenna [166]. The antenna has an integrated LNA of 27 dB gain, to compensate for transmission line losses. A 5 m coaxial cable connects it to the receiver. The output is a dual RS-232 transceiver. The first serial line port connects to the Priamos DSP engine to synchronise the cross-correlation and data time-stamping functions. The second serial port was initially connected to the host to evaluate the product and removed eventually. The GPS data are routed through the FPGA to host via the USB or LAN port. Re-configuration of the GPS receiver is achieved by modifying the 8 Mb on-board Flash memory.

4.7 Experimental Results for the RF Receiver

A 4.02 mV, 38.2 MHz sinewave input is connected to the input of the receiver, as in Fig. 4.8. The scale is 2 mV/div and 50 ns/div. The input in frequency domain is in Fig. 4.9. The scale is 10 dB/div and 6.25 MHz/div. The ISA level commands 1021h and 1024h yield to Cali = 0, Bypass = 1 and Rfbyrl = 1.

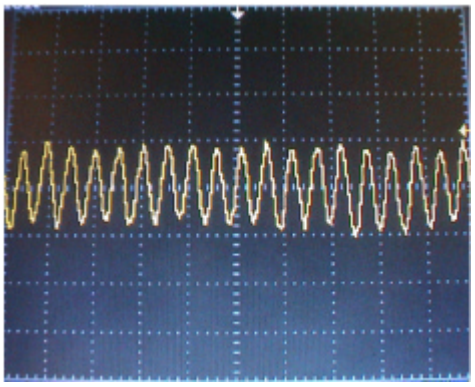


Figure 4.8 Time Domain Sinewave Input to the Receiver.

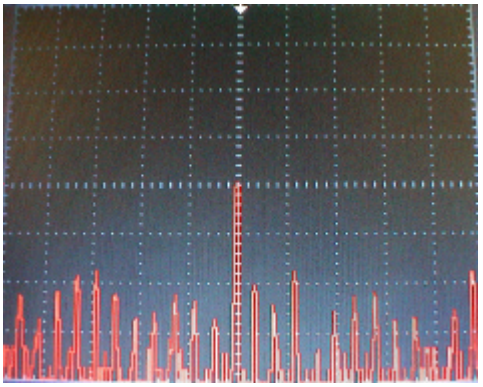


Figure 4.9 Frequency Domain Sinewave Input to the Receiver.

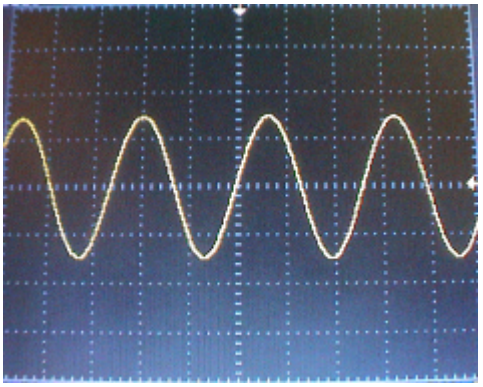


Figure 4.10 Time Domain LPF Output.

The time domain waveform measured on pin 4 of the RF transformer is Fig. 4.10. The scale is 50 mV/div and 10 ns/div. The 38.2 MHz sinewave LPF output has a Vpp value of 148 mV. The results in frequency domain are in Fig. 4.11. The scale is 10 dB/div and 6.25 MHz/div. The calculated gain based on the rms results is 31.32 dB.

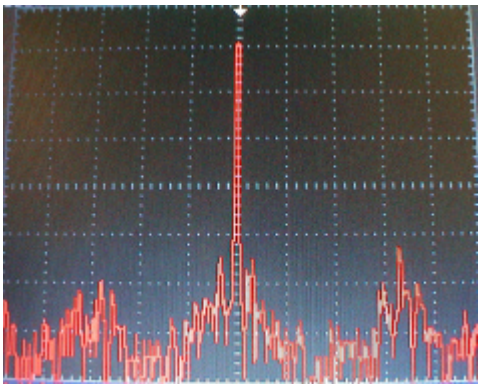


Figure 4.11 Frequency Domain LPF Output.

The gain for the subsystem chain is also derived by eq. (4-1):

$$G = 32\ dB - (0.02\ dB + 0.02\ dB + 0.31\ dB + 0.3\ dB + 0.02\ dB) = 31.33\ dB \qquad (4\text{-}1)$$

where, 32 dB is the set gain of the PA, 0.02 dB x 3 the loss through the three RF relays, 0.31 dB the loss through the PA circuit and 0.3 dB the loss through the LPF.

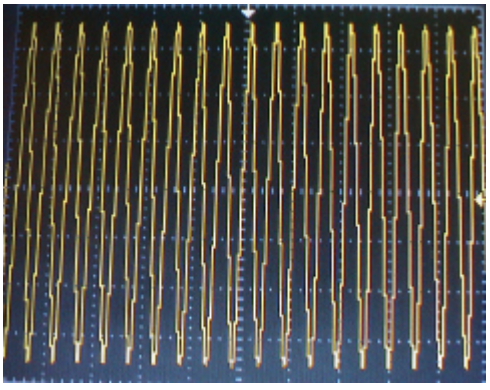


Figure 4.12 RF Transformer LPF Output.

The 38.2 MHz time domain output at pins 1 or 3 of the RF transformer is in Fig. 4.12. Vpp is 71 mV. The scale is 10 mV/div and 50 ns/div. The loss through the RF transformer for

both balanced outputs is 0.359 dB. The common mode (CM) output of the ADC connects to pin 15 of the AGC and is 1.55 V as in Fig. 4.13. The scale is 500 mV/div and 1 us/div.

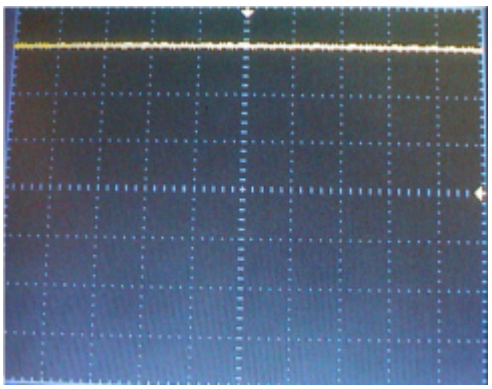


Figure 4.13 Common Mode Voltage.

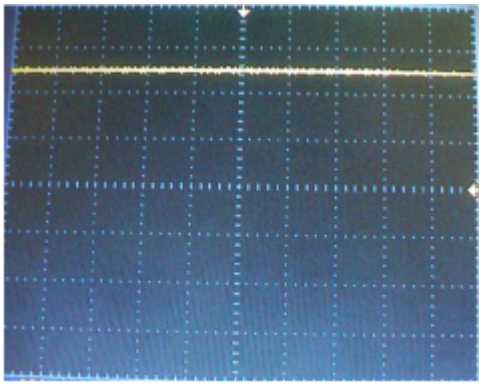


Figure 4.14 Setting the AGC Output Swing.

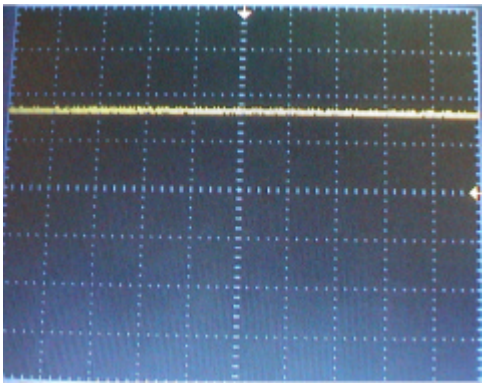


Figure 4.15 Setting the AGC Gain.

The voltage output swing of +/- 2V requires VMAG to be 0.5 V as in Fig. 4.14. The scale is 200 mV and 1 us/div. Prior testing, the gain was 22 dB by setting VDBS to 0.84 V as in Fig. 4.15.

The scale is 500 mV/div and 1 us/div. However, 22 dB saturates the receiver in this test and it was reduced to 6 dB. The 38.2 MHz time domain output at AGC pins 12 (INP1) or 13 (INM1) is in Fig. 4.16. The 38.2 MHz AC component has Vpp of 142 mV, superimposed on the DC common mode voltage. The scale is 500 mV/div and 50 ns/div. The reference ground is almost three y – axis unit steps lower than the channel's mean component in the snapshot.

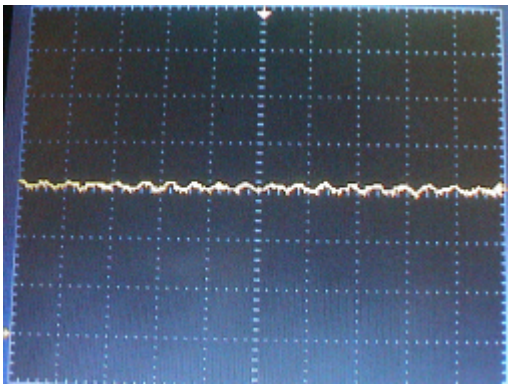


Figure 4.16 AGC LPF Output.

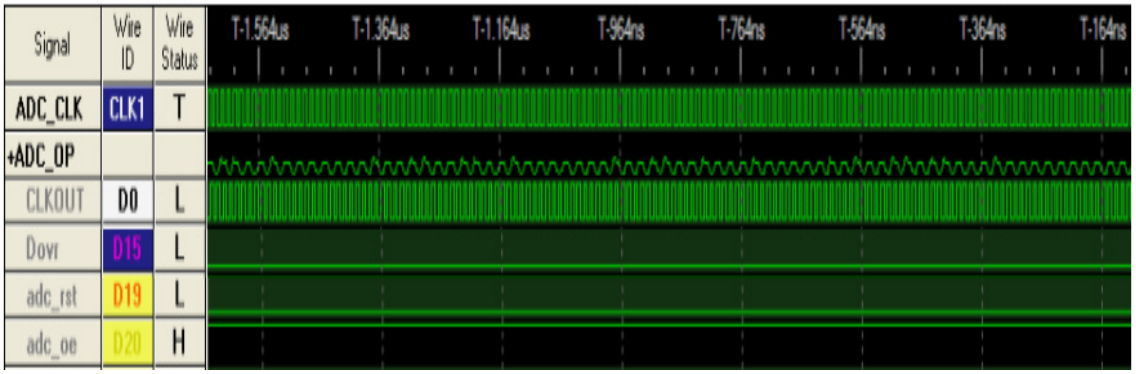


Figure 4.17 ADC LPF Output.

The ADC is programmed via the FPGA by the host PC to have ADC_RST = 0, ADC_OE = 1, PDOWN = OFF and DLL = ON, as in Fig. 4.17. The snapshot is produced by connecting the major digital inputs and outputs of the ADC to a 500 MSPS digital logic analyser. The ADC_CLK is the 95.5 MHz output of the master oscillator, programmed by the FPGA. The ADC_OP bus is the 14-bit ADC output data bus. The bus is combined and set to analogue display. CLKOUT is the 95.5 MHz clock output of the ADC to synchronise with the FPGA. DOVR is the data overflow output, zero during the test.

The ISA level commands 1021h and 1023h yield to Cali = 0, Bypass = 0 and Rfbyrl = 0. The sinewave of Vpp = 4.02 mV is routed through the BPF. The time domain waveform measured on pin 4 of the RF transformer is Fig. 4.18. The scale is 20 mV/div and 50 ns/div. The 38.2 MHz sinewave BPF output has a Vpp value of 120.4 mV. The results in frequency domain are in Fig. 4.19. The scale is 10 dB/div and 2.5 MHz/div. The voltage gain is 29.53 dB.

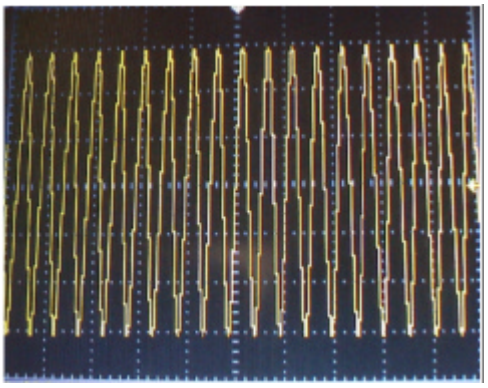


Figure 4.18 Time Domain BPF Output.

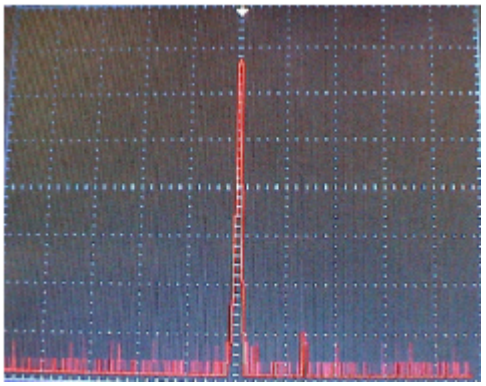


Figure 4.19 Frequency Domain BPF Output.

The gain is also derived by eq. (4-2):

$$G = 32\ \text{dB} - (0.02\ \text{dB} + 0.02\ \text{dB} + 0.31\ \text{dB} + 2.1\ \text{dB} + 0.02\ \text{dB}) = 29.53\ \text{dB} \qquad (4\text{-}2)$$

where, 32 dB the PA gain, 0.02 dB x 3 the loss through the three RF relays, 0.31 dB the PA loss and 2.1 dB the BPF loss. The 38.2 MHz time domain output at pins 1 or 3 of the RF transformer is in Fig. 4.20. Vpp is 57.8 mV. The scale is 10 mV/div and 50 ns/div. The loss through the RF transformer for the balanced outputs is 0.353 dB.

The AGC gain is set by the host to 8 dB to compensate for the 1.8 dB gain difference between the LPF and BPF signal paths. The 38.2 MHz time domain output at AGC pins 12 (INP1) or 13 (INM1) is in Fig. 4.21. The 38.2 MHz AC component has Vpp of 145.2 mV, superimposed on the DC common mode voltage. The scale is 500 mV/div and 50 ns/div. The reference ground is three y - divisions below the centre. The ADC is programmed in the same mode as in the previous test and the logic analyser's results are in Fig. 4.22.

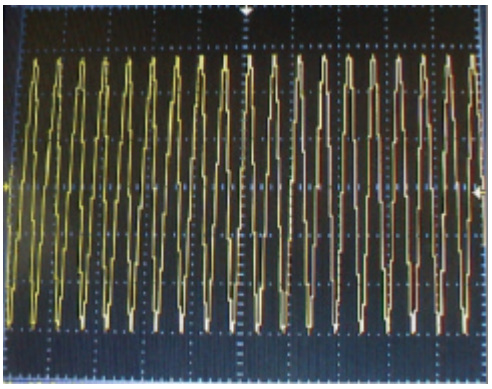


Figure 4.20 RF Transformer BPF Output.

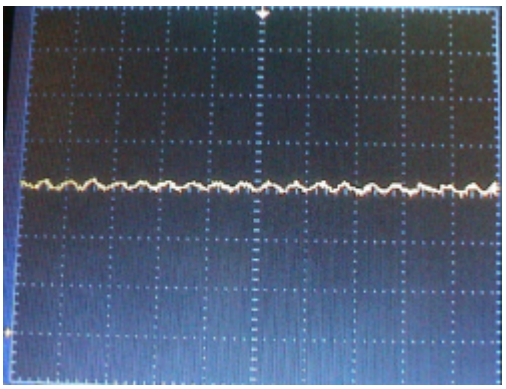


Figure 4.21 AGC BPF Output.

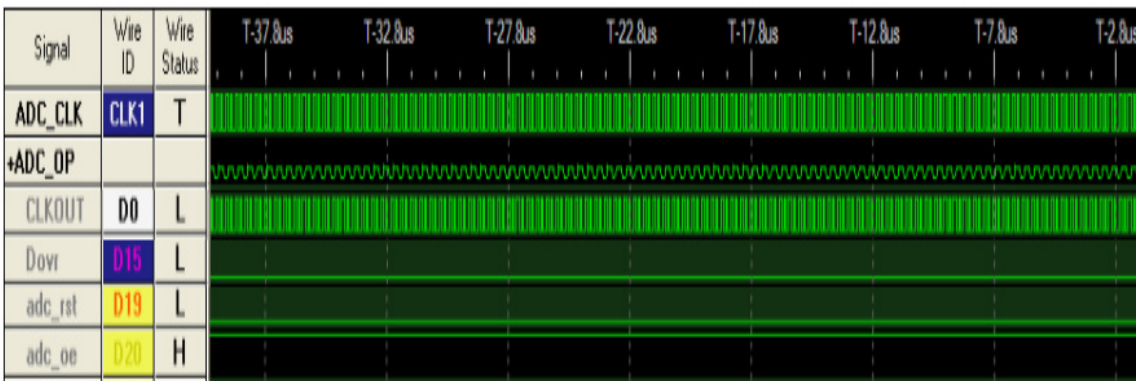


Figure 4.22 ADC BPF Output.

The ISA level commands 1022h and 1024h set Cali = 1, Bypass = 1 and Rfbyrl = 1. The system switches to calibration. The frequency response at the NC203 cathode is in Fig. 4.23. Any AC response is not visible by the spectrum analyser. The scale is 20 dB/div and 2.5 GHz/div. A DC component of 8.86 V exists in the DC domain, as in Fig. 4.24. The scale is 2 V/div and 100 us/div. The output of the noise generator at C2 is in Fig. 4.25. Vpp is 2.13 mV. The scale is 2 mV/div and 1 ms/div. Four overlapped samples are averaged.

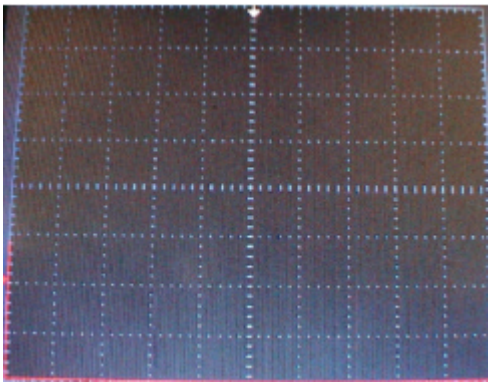


Figure 4.23 NC203 Cathode Frequency Domain Response.

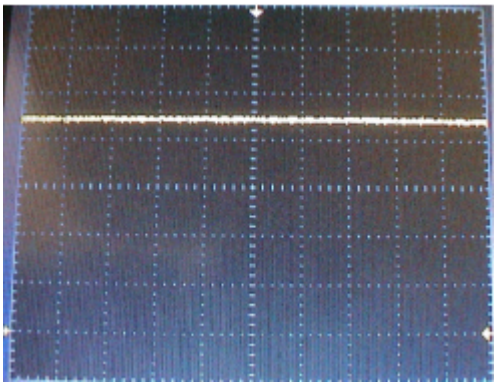


Figure 4.24 NC203 Cathode Time Domain Response.

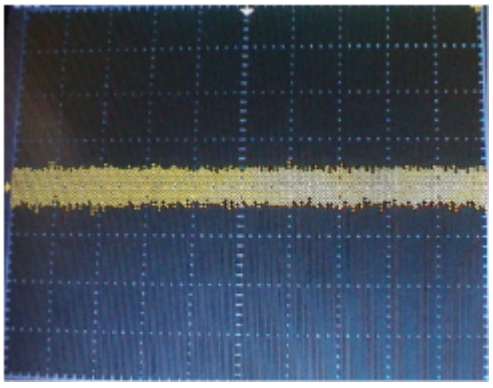


Figure 4.25 Noise Circuit Time Domain Output.

The frequency response at the PA output is in Fig. 4.26. The scale is 10 dB/div and 50 MHz/div. The 60 MHz LPF action is in Fig. 4.27. The scale is 10 dB/div and 50 MHz/div. The voltage at the RF transformer's input is in Fig. 4.28. Vpp is 70 mV. The scale is 20 mV/div and 50 us/div. The voltage gain is 30.33 dB. Eq. (4-1) is verified since the attenuator is set to 1 dB.

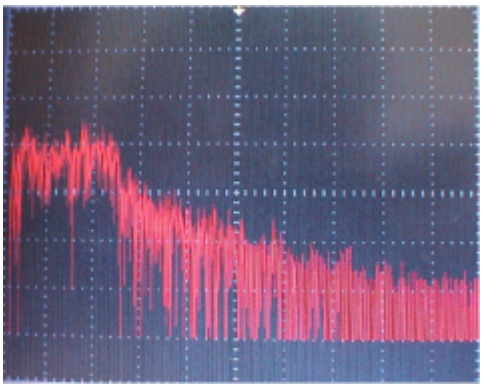


Figure 4.26 Frequency Domain PA Output.

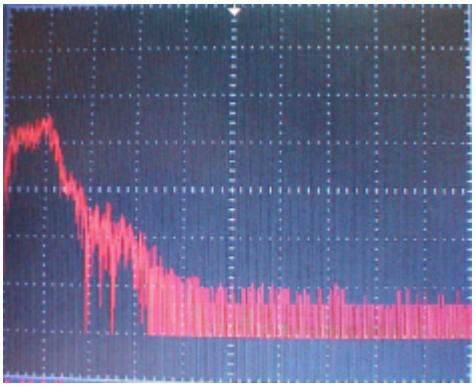


Figure 4.27 Frequency Domain LPF Output.

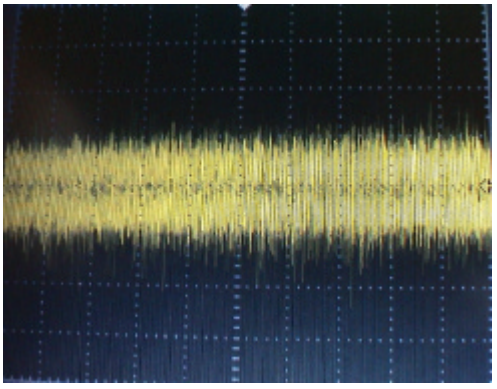


Figure 4.28 RF Transformer LPF Output.

The RF transformer's output is in Fig. 4.29. Vpp is 67.2 mV. The scale is 20 mV/div and 50 us/div. The loss is 0.354 dB. During the first experiment using the LPF signal path, the AGC gain was 6 dB. Compensating for the 1 dB loss through the attenuator, the AGC gain is set to 7 dB. The waveform at the AGC output is in Fig. 4.30. Vpp is 150 mV, superimposed on Vcm. The scale is 500 mV/div and 1 ms/div. The logic analyser's output is in Fig. 4.31.

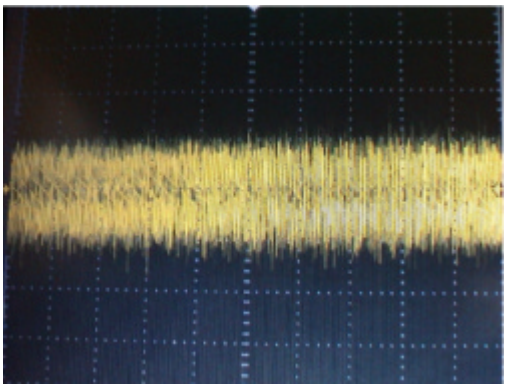


Figure 4.29 RF Transformer Output.

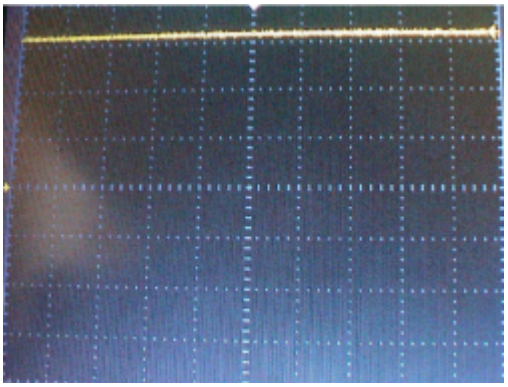


Figure 4.30 AGC LPF Output.

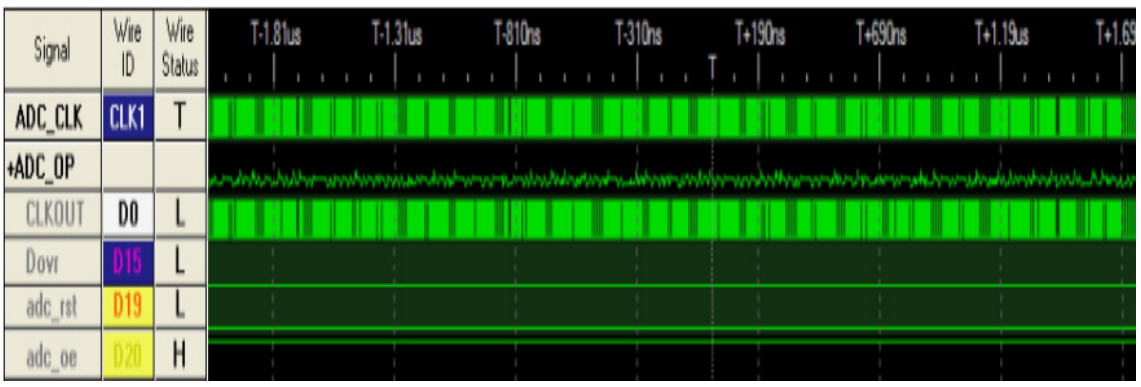


Figure 4.31 ADC LPF Output.

The ISA commands 1022h and 1023h in machine language are issued setting Cali = 1, Bypass = 0 and Rfbyrl = 0. The system is in calibration mode and the noise source is routed through the BPF. To compensate for the 1 dB attenuator's loss the AGC gain is set to 9 dB. The input to the RF transformer is 56.9 mVpp, while the output 54.6 mVpp. Four overlapped samples are averaged. The output of the AGC is 154 mVpp superimposed on Vcm. The logic analyser's output is in Fig. C.9.

The system's auto-recovery from ADC saturation that would occur during type III and IV SREs is tested next. The previous experiment is repeated for a varying AGC gain, e.g. 30 dB. The ADS5500 output is monitored by the logic analyser in Fig. C.10. The ideal AGC output is 1.73 Vpp at 30 dB superimposed on Vcm. The AGC ouput swings along both FS edges. Similarly, the ADC output swings along FS and is in saturation most of the time by observing the Dovr output.

An 11 states state machine is created for this test inside the FPGA to autonomously adjust the AGC gain to avoid saturation. A time variant counter synchronises auto-recovery and creates transition intervals between 10.47 ns and 209.4 ns. The state machine is not software controlled, in contrast to the Priamos final master controller. Working on the physical layer allows faster programming of the AGC and hardware reaction within ns, as in Fig. C.11. SREs may last for hours and software control is adequate.

At T – 4 us the ADC_OP is 154 mVpp at 9 dB gain. The state machine issues the 4 – cycle ISA equivalent 1001h in machine language Load_RDAC1 command, driving the digital amplifier's SPI interface circuits. The RDAC1 output is set to 1.08 V for an AGC unloaded gain of 36 dB, corresponding to a loaded gain of 30 dB.

At T – 3.925 us the ADC output enters saturation mode for 104.7 ns. The controller detects the overflow and issues the final system's ISA equivalent 4 – cycle 100Ch EEMEM0_RDAC1 and 100Bh NOP commands. The first command loads the 9 dB setting previously saved to the nonvolatile EEMEM0 register. The EEMEM0_RDAC1 command leaves the device to the read program state. The no operation (NOP) command executes, returning the device to idle.

4.8 Priamos RF Receiver Unit

The Priamos receiver prototype yielded to a four-electrical-layer RF high-speed PCB. 50 R impedance matching and high-frequency rules apply. The RF PCB top- and bottom-sides are in Fig. C.12 and C.13, respectively. The fully assembled unit is presented in Fig. C.14. The input on the right is a 50R BNC type connector coaxial cable. The top 40-way IDC ribbon cable on the left digitally controls the receiver. The bottom ribbon cable connects the datapath signals to DSP engine of the next chapter.

4.9 Conclusion

The chapter described the RF receiver and peripheral hardware design for Priamos. The design of a crossed-dipole antenna at 38.2 MHz is presented in App. B. The antenna was modelled using the Mininec electromagnetic simulator, which is based on the method of moments (MoM) numerical technique. The antenna was 3-D modelled, the vertical and horizontal normalised radiation patterns were obtained and a 3-D dimensional radiation pattern was produced. From the antenna's normalised vertical radiation pattern the maximum gain is 5.8 dB for 0 deg zenith angle. The antenna has a constant gain for all azimuth angles. The half-power beam width is 83.36 deg.

The 50R matched output of the antenna connects either to the 38.2 MHz PA or the 1 – 60 MHz PA. Both PAs are based on the MMIC MSA-0886 with gain of 32 dB, NF of 3.05 dB, OIP3 of 24.5 dBm and IM3 of -277.9 dBm. The group delay is approximately 300 ps. Several other PA designs were considered prior the selection of the MSA-0886, based on single and double tuning circuits. However, their performance was not suitable for Priamos.

The 1- 60 MHz PA connects to a 60 MHz cut-off frequency LPF. The 37.7 – 38.7 MHz preamplifier's output connects to a 38.2 MHz BPF of 1 MHz bandwidth. Several architectures were investigated for their performance and cost. Additionally, two types of BPF were simulated for bandwidths of 250 KHz and 1 MHz. The 250 KHz bandwidth BPF requires advanced construction experience due to the filter's sharp roll off and the ratio of centre frequency to bandwidth is low. It is difficult to build a BPF of less than 1% ratio.

However, the 250 KHz design restricts the system from experimenting with the variable bandwidth option. Riometers typically target bandwidths between 15 – 250 KHz, which is increased to 1 MHz by the presented system. The observation resolution depends on the narrowness of the beam. In phased-array systems, lowering the bandwidth to less than 100 KHz, increases spatial resolution. Nevertheless, the temporal resolution is increased. On the contrary, in the Priamos case the large half-power beam width of the antenna does not allow collection of higher spatial resolution data by reducing the bandwidth to less than 100 KHz.

A digital amplifier was designed to digitally control in real-time the receiver's second gain stage. The AGC matches the LPF and BPF output to ADC's input impedance. The presented design also converts the single-ended output of the LPF or BPF to a differential input. A differential input to the 125 MSPS ADC is required to meet the performance of the ADS5500 device.

Selection of the master oscillator device was crucial to the system's performance. Two ICS525-02 ICs are used. The first ICS525-02 device is configured manually, with a set of dual in line switches, to produce a 25 MHz reference clock signal. The second device is programmed in real-time by the FPGA to produce the required sampling frequency.

The GPS receiver instrumentation manages the demand for accurate UTC time, data time-stamping, accurate 1 pulse-per-second for the cross-corellator and geographical position.

The next chapter is dedicated to the design and hardware implementation of the Priamos DSP engine.

Chapter 5.

Novel Programmable Riometer for in-depth Ionospheric And Magnetospheric ObservationS (PRIAMOS) Using Direct Sampling DSP Techniques:

DSP Engine Hardware Design

5.1 Introduction

The chapter describes the hardware design of the Priamos DSP Engine. Hardware implementation of a digital FIR BPF operating at 95.5 MHz sampling frequency is considered first. The FIR BPF tuned to 38.2 MHz exhibits 250 KHz bandwidth. The number of coefficients is determined and symmetrical filter architecture is proposed. The excessive DSP power requirements indicate that the implementation is impossible into any commercial FPGA or DSP device. A DDC stage is required before the FPGA or DSP.

Three different system architectures were investigated and the optimum is developed. The first scenario requires the TMS320C6416-1GHz DSK to be interfaced by seven other prototype boards, including the RF Receiver of the previous chapter. The limited number of I/Os allows partial control over the system and most of the programmable features are disabled, including the on-board SDRAM. A peripheral co-processor on the HPI bus is still required to fully control the system.

A custom DSP-based with FPGA co-processor computer architecture is seriatim considered. Programming the devices is in three languages, two design flows and two programming styles. Testing and debugging requires extra hardware and effort when SDR functions involve real-time bi-directional routing of significant amount of data between the host and the DDC or RF receiver's programmable devices, via six computer engineering interfaces.

The co-processor considered performs datapath processing adequately, but lacks the unified software and hardware flexibility required. Considering the resulting hardware design complexity and overall prototyping cost, an FPGA-based solution is evaluated and a design is presented.

The FPGA-based DSP Engine unit supports over 300 SDR commands in hardware. The eight implemented mega-function modules programme or reconfigure the FPGA, RF Receiver Unit, GPS receiver, master oscillator, 16 Mbps SRAM and glueless USB 2.0 or 10/100 Mbps Ethernet interfaces.

Programmable features include: dual-DDC processing, auto-correlation, sampling frequency up to 250 MHz, integration time, UTC real-time clock (RTC) timekeeping, UTC data timestamping, long data timestamped storage etc. The DSP Engine Unit is independent of the antenna being used and other space physics instrumentation projects are quickly prototyped.

5.2 Digital Finite Impulse Response Filter Design

The implementation of a digital BPF [168] tuned to 38.2 MHz and 250 KHz BW was first investigated. A thorough investigation into digital filtering was conducted and the major results are presented.

Digital filters change the signal shape and amplitude-frequency relationship. FIR filters are more likely to have a linear phase response. They are easier to implement, since they provide direct hardware implementations. The design involves calculating the coefficients, realising the structure, analysing the 14-bits wordlength effect on performance and hardware implementing the filter.

For 250 KHz BW, the passband is between 38.075 and 38.325 MHz. The low and high passband edge frequencies are calculated by eq. (5-1):

$$PB_L = \frac{38.075MHz}{95.5MHz} = 0.39869$$
$$PB_H = \frac{38.325MHz}{95.5MHz} = 0.40130 \qquad (5\text{-}1)$$

Typical filter designs exhibit passband deviation of 0.05. The passband ripple equals:

$$As = 20\log(1 + 0.05) = 0.42\ dB \qquad (5\text{-}2)$$

For an optimum filter the stopband attenuation As is close to 80 dB. Therefore, the stopband deviation (ds) is the antilog of -4, as formulated in (5-3).

$$As = -20\log(ds) \Rightarrow ds = 10^{-4} \Rightarrow ds = 0.0001 \qquad (5\text{-}3)$$

The transition width is calculated by eq. (5-4):

$$Tw = \frac{50KHz}{99.5MHz} = 0.000521376433 \qquad (5\text{-}4)$$

The transversal structure yields to efficient FPGA or DSP implementations [169]. FIR filters are typically designed using the window method. For a stopband attenuation of 80 dB, the Kaiser Window function is appropriate, with b = 8. The implemented window function is in eq. (5-5):

$$f_{kaiser} = \frac{Io(\beta\sqrt{(1-[\frac{2n}{(N-1)^2}])}}{Io(\beta)} \qquad (5\text{-}5)$$

Manual calculation of the Kaiser function coefficients requires significant effort for a high order filter. Scientific software [170-171] is used, such as the Matlab FIR design package to simulate different filter configurations.

Using 65 coefficients and considering 14-bits quantisation effects the achieved passband and stopband attenuation is 0.0009705 and 64.858 dB, respectively. BW is 7 MHz. The filter design does not meet the specifications due to the high centre frequency, low BW, low transition width and small number of coefficients. The order was increased to 240, 14-bits quantisation effects were considered and the filter's performance is in Fig. 5.1.

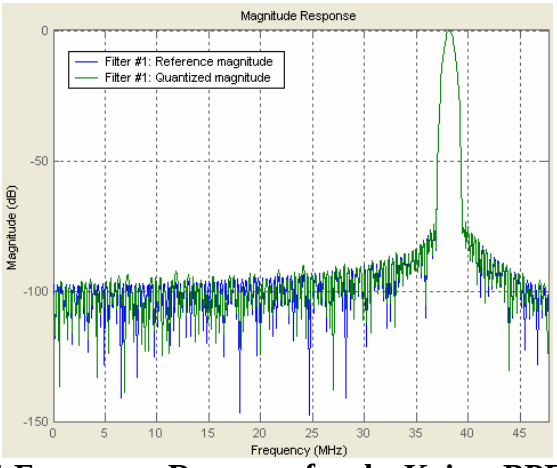


Figure 5.1 Frequency Response for the Kaiser BPF (N=240).

The specifications are not fully met. The bandwidth is 620 KHz and the transition width is 1.1 MHz. After a trial-by-error procedure, the optimum frequency response is in Fig. 5.2. The filter has 9568 coefficients and yields to the best possible configuration. The bandwidth is 250 KHz and the transition width is 50 KHz. The minimum passband ripple and stopband attenuation is 95 dB.

The filter is stable and designed as a direct form FIR [169] in Fig. 5.3. The delay chains, zero gain, unity gain and -1 gain are optimised.

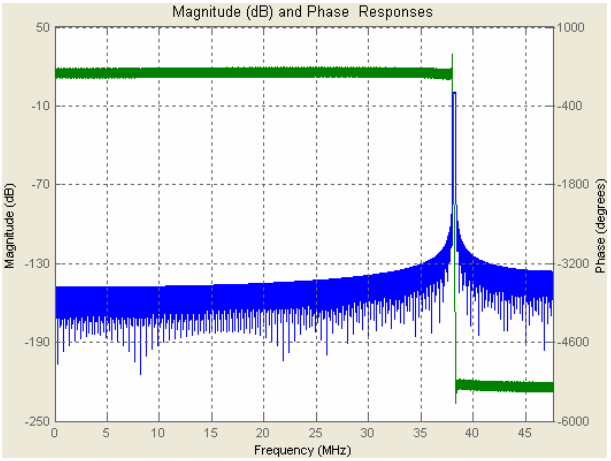


Figure 5.2 BPF Frequency and Phase Response (N=9568).

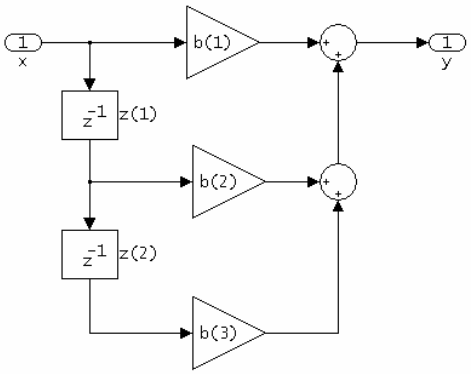


Figure 5.3 Direct Form FIR BPF Implementation.

The filter can be transformed into a series of other architectures. Each architecture presents advantages and disadvantages. Suitable architectures are the transposed, antisymmetric and symmetric [172]. Hardware resources utilisation and device performance is optimised using the symmetric architecture. It reduces the number of required coefficients by a factor of two by taking advantage of the filter's symmetrical properties. Calculations estimate the DSP power to implement the filter.

For a sampling frequency of 95.5 MHz the DSP has 10.47 ns to process each sample. The FIR filtering performance determines the required power, since the DSP performs filtering most of the time.

For a 20^{th} order filter, 20 MAC instructions are executed on every sample [173]:

$$20 * 95.5 \text{ MHz} = 1910 \text{ MIPS} \quad (5\text{-}6)$$

Additional memory moves and repeat loops increase the processing power to:

$$2 * 1910 \text{ MIPS} = 3820 \text{ MIPS} \quad (5\text{-}7)$$

Power is calculated by integrating the signal over 1 s and 1 MAC instruction per sample is needed. Overflow checking requires 1 or 2 MIPS. The minimum DSP capacity equals:

$$3820 + 1 + 2 = 3823 \text{ MIPS} \quad (5\text{-}8)$$

The filter's type and order dominates the DSP power calculations. If the symmetrical BPF is implemented 4784 coefficients are required, resulting to:

$$2 * (4784 * 95.5 \text{ MHz}) + 3 = 913747 \text{ MIPS} \quad (5\text{-}9)$$

DSP power is also derived by implementing the FIR library functions. DSP libraries include C-callable functions, optimised [174] using assembly language [175]. The C64x DSP family has four FIR functions, namely DSP_fir_gen, DSP_fir_r4, DSP_fir_r8 and DSP_fir_sym. If the filter functions are implemented with 9568 coefficients, the number of cycles to produce the first 200 outputs is 478965, 478809, 478416 and 299776, respectively.

The implementation of the symmetrical BPF using the DSP_fir_sym function and 4784 coefficients requires 300,000 clock cycles to produce the first 200 outputs. This is referenced to 1500 clock cycles to produce the first output.

The FIR BPF is impossible to be implemented into any of the commercial DSP devices. A DDC must be connected prior the DSP, eliminating the BPF's excessive hardware resources implementation requirements.

5.3 Digital Down Converter Selection and Modelling

A DDC device performs a series of intensive DSP functions, such as RF down conversion to baseband and FIR filtering. A possible candidate is the Alcatel's DDC [176]. TI, Philips, Siemens [177] and other companies produce similar chips [178-179]. For performance and compatibility related purposes a TI device is recommended. TI produces the GC5016 (150 MSPS, 115 dB SFDR, 250 mW), GC1012B (100 MSPS, 75 dB SFDR, 850 mW) and GC4016 (100 MSPS, 115 dB SFDR, 115 mW). The ADC samples up to 125 MSPS. GC5016 is selected coupling the ADC's capabilities.

GC5016 performance is higher when processing complex signals [180]. CN amplitude and phase could have been extracted earlier in the design. A complex input would have been used, if the sampling requirements were lower. For instance, the 80 MSPS ADS5410 ADC produces I and Q channel information. However, ADS5550 has a single real 14-bits parallel output and GC5016 is configured to accept a real input.

The Matlab Simulink model of Fig. 5.4 evaluated Priamos performance using TI's GC5016 reference design. The system's NF of 3.1 dB was added as thermal noise.

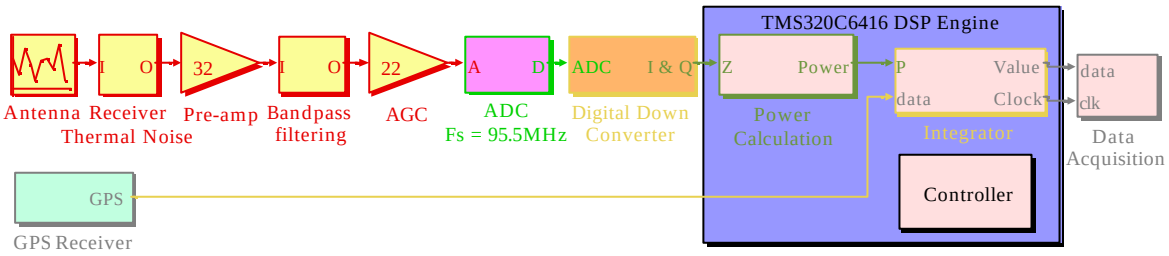


Figure 5.4 Priamos Basic Simulation Model.

Down conversion of 38.2 MHz CN to baseband is achieved by the numerical controlled oscillator (NCO) and mixer circuits. The NCO produces sine and cosine functions by sampling the first quarter of a sinewave only. The CIC, CFIR, PFIR and resampler filters provide the LPF functionality.

Further details about the feasibility study and performance of the initial DSP-based Priamos version using GC5016 are in [181]. Sections 5.4 – 5.6 justify the engineering decisions taken before mitigating from a DSP- to an FPGA-based system.

5.4 Digital Signal Processor Selection

For compatibility purposes a TI device is recommended. Fixed-point DSPs handle numbers in software, increasing the programming difficulty. Floating-point DSPs use hardware resources to handle numbers, increasing the complexity and cost of the processor. Fixed-point accuracy is sufficient for Priamos.

The C64x fixed-point family is an extension of C62x in terms of performance and additional peripherals. The C64x devices feature operation at 1 GHz, 8000 MIPS, 4000 MMACS and 1.06 W power consumption. Peripherals include 3 McBSP, 32 bits/33 MHz PCI, 64-channel DMA, 16 - 64-bits EMIF, UTOPIA, 32-bits HPI etc. TMS320C6416 [182] at 1 GHz provides 8000 MIPS.

5.5 Prototyping Priamos using the C6416 DSK

The TMS320C6416-1 GHz DSP was evaluated using the C6416 DSP Starter Kit (DSK) [183]. External memory interface (EMIF) A bus interfaces the DDC. The host peripheral interface (HPI) connects to a custom UART board for data transfers. Data logging is not possible through the USB port, since it is dedicated to JTAG emulation and communication with the Code Composer Studio (CCS). Software programs and processed data are placed in the unified 32-bits address space.

Each EMIF addresses one of the four chip enable spaces (CE0-CE3). The SDRAM chip writes to CE0 of EMIF A. The Altera EPM3128TC100-10 CPLD and flash memory are mapped to CE0 and CE1 of EMIF B. Daughter-cards are on EMIF B CE2 and CE3.

5.5.1 FIFO Interface Between the DDC and DSP

The 373.04 KSPS DDC output connects to the 250 MHz EMIF A. The FIFO buffers data to be read in burst mode by DMA transfers [184]. The SN74V273 [185] dual-port, glueless [186] FIFO operates in standard and first-word fall-through (FWFT) modes. It is the only asynchronous EMIF device. FIFO is set to FWFT mode. The half-full (HF) flag triggers DMA transfers. The 16-bits AO [15:0] and ACK DDC outputs connect to FIFO in Fig. 5.5. The SYNC input has setup time (tsu) > 2 ns and hold time (thd) > 0.5 ns. The outputs maintain the previous value for a minimum of 1 ns. Data are valid for 5 ns after the clock's rising edge. There is no delay between ACK and A0 [15:0].

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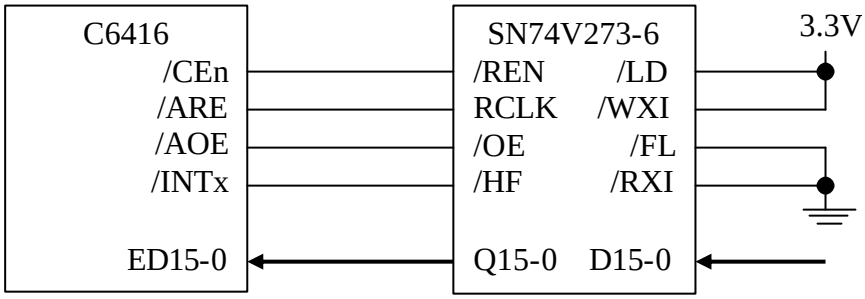


Figure 5.5 Glueless SN74V2x5-to-EMIF Interface.

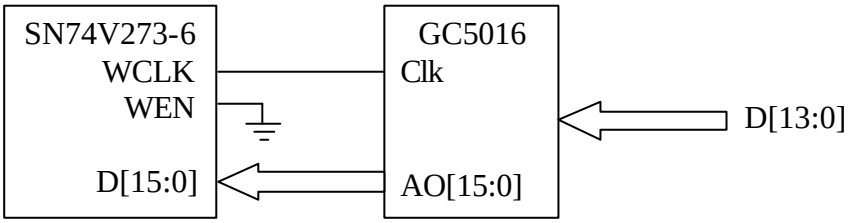


Figure 5.6 DDC-to-FIFO Interface.

For the SN74V273 -6 speed tsu = 1.5 ns and thd = 0.5 ns. ACK has cycle time of 2.68067767 us. The DDC output data are valid for at least 5 ns before the clock's rising edge and at least 1 ns after. Consequently, there are no concerns with the setup time of the FIFO inputs. The DDC provides output data 16.5 cycles after the first sample at its input. To avoid filling the FIFO with data, while the DSP is initialising, a DSP pin holds the FIFO in reset. When the DSP is ready, the pin is released and the FIFO starts operating.

5.5.2 UART Data Interface

The only computer interface (USB) configures and debugs the DSK. McBSP0 interfaces to UART by modifying the serial control registers [187]. The adapter in Fig. 5.7 consists of a SN75LV4737A [188] RS232 line driver/receiver [189] in serial port mode [190].

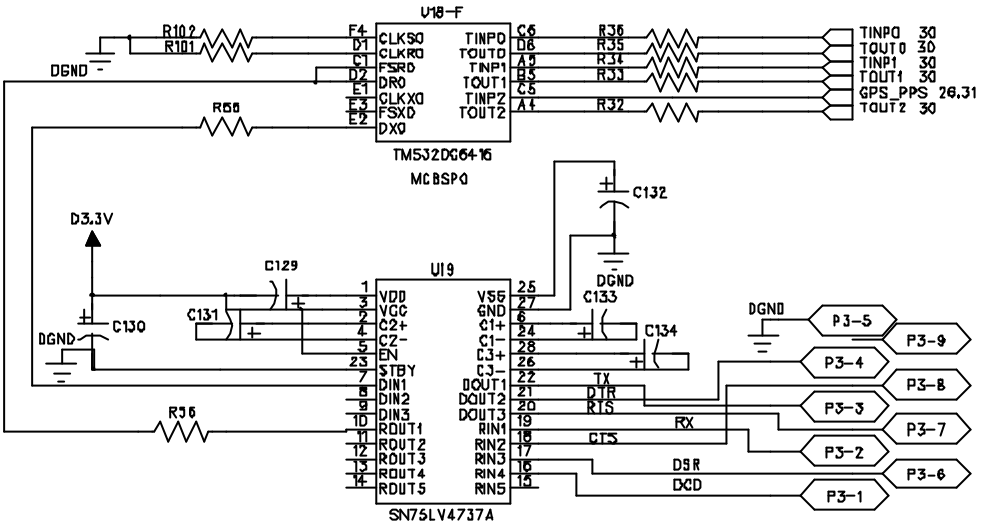


Figure 5.7 UART Data Interface.

5.5.3 DSK-Based Priamos Prototype Considerations

Prior to the development of the RF receiver the preliminary prototype requires 10 boards. The number reduces to 7, consisting of the RF receiver, DDC, FIFO, Master Oscillator, GPS, DSK and UART boards. Most of the programmable features are set to default values, since the DSK has not enough I/Os. The external SDRAM on EMIF A is disabled to avoid bus conflicts. The system operates a real-time data transfer scheme. The GPS receiver connects to the PC and data time-stamping occurs during data logging.

An external controller on the HPI bus is required to fully control the system. Multi-board systems have lower reliability factors. Power consumption is higher, due to the unnecessary components of the DSK board. Separate software is required for configuring and debugging the card (CCS), and for data logging (C/C++). These concerns lead to a custom DSP-based with FPGA co-processor support design.

5.6 DSP with FPGA Co-Processor Priamos Design

The top-level board design is in Fig. 5.8. Due to the connections intensity a limited number exists at the top-level. Two 40-pin IDC connectors achieve the data and control communication between the DSP and RF receiver boards. The inputs are buffered before reaching the DDC. The DDC outputs are stored in the FIFO. The FIFO is accessed by EMIF A bus, as in Fig. D.1.

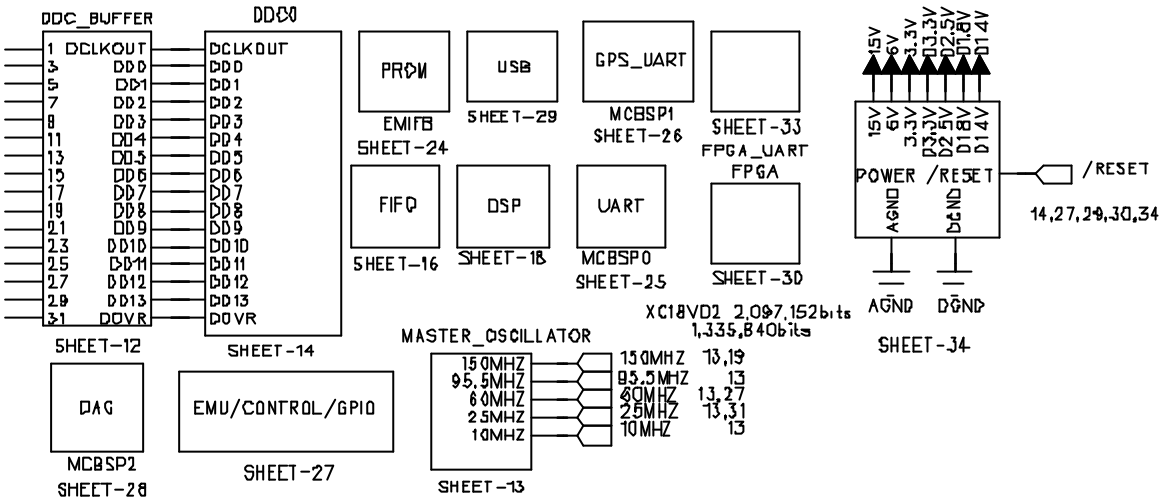


Figure 5.8 Priamos DSP Board Top-Level Schematic.

The 32-bits HPI interface performs bi-directional transfers between the DSP and FPGA. Both devices have privileges to read and write to a register set of the other device. The XC2S200 FPGA [191] in Fig. D.2 controls and programs the master oscillator, DDC, ADC, DSP timers, FPGA UART (for diagnostics) and GPS UART. It electronically switches between calibration, BPF and LPF inputs.

The DSP controls and programs the digital amplifier, FIFO, USB (data logging), UART (data logging) and the GPS UART. The EMIF B interface sets the DSP operation mode and provides bi-directional communication to the USB 2.0 controller. The USB 2.0 interface is implemented using the CY7C68001 controller from Cypress [199].

5.6.1 Software Design and Analysis

The GC5016 ACK output rate is 373.04 KSPS, filling the FIFO in 43.90912 ms. Each 36-bits FIFO location contains the parallel outputs I (DDC's A0 [15:0]), Q (B0 [15:0]), AFS and BFS flags. SD_INTA on EDMA channel 3 is submitted every 43.90912 ms [198], triggering EMIF A AED [31:0] (AED [15:0] for A0 and AED [31:16] for B0 in Fig. D.1) to transfer the data block to EMIF A L2 SRAM CE0 (80000000 - 80003FFF) in 65.564 us. For this operation the pipeline consists of 8 stages [182].

A software loop loads the 32-bits I and Q combined value to register file A. The .M1 unit performs a dual 16-bits MAC operation on I and Q for the I channel calculation, which approximates 2000 million MACs per second (MMACS) near the loop exit point. The Q channel is 0 in auto-correlation. The software loop takes 32775 ns or clock cycles for an 8 stage CPU load pipeline, although MAC has a 7 stage pipeline. The total process requires 98339 clock cycles. The result is temporarily stored in the accumulator. Allowing the option for double-buffering, the accumulator also stores the intermediate results into L2 SRAM CE0 (80008000 - 8000BFFF). Timer 2 accepts the GPS 1 pps on pin C5, programs the integration time in 32-bits resolution and triggers the .M1 unit to store the integrated result to CE0 (80010000 – 80013FFF). The FPGA controls Timers 0 and 1, and also connects to the 1 pps signal. Timer 1 is used for clock recovery during loss of GPS synchronisation.

43,810,781 clock cycles remain until SD_INTA is resubmitted. The FPGA's DSP interface is updated by first updating the HPI registers. The medium priority transfer request, automatically submitted to EDMA, is real-time processed. Programming the master oscillator, ADC, DDC and RF switching is achieved by submitting a fixed-address single-element request. The same request is submitted for accessing the mapped status registers in the FPGA. Software interrupts for reprogramming the DDC lead to the auto-increment HPI address registers update. 32-bits bursts, while HD5 = 1, are transmitted to the FPGA registers until the configuration length is reached. Data time-stamping occurs by submitting REVT 1 interrupt and decoding the streaming GPS data on McBSP 1. The auto-correlated results are concatenated with UTC in CE0 (80014000 – 8FFFFFFF). EMIF B SD_INTB interrupt initiates a real-time USB 2.0 host transfer.

5.6.2 DSP with FPGA Co-Processor Design Considerations

The design encompasses two programming styles. The DSP is programmed by software sequential execution, while the FPGA supports parallel processing. Software is developed using CCS (C and assembly) and Xilinx (VHDL) design flows. C/C++ is used for data logging. TMS320C6416, GC5016, XC18V02 PROM and XC2S200 form a JTAG emulation and configuration chain. GC5016 is not configured through JTAG. Its configuration files are opened in software and passed to DSP. The DSP HPI interface transfers data to the FPGA, triggering the DDC interface to program the device.

The XC2S200 has embedded multipliers that perform MAC operations equally well and, as explained in chapter 2, recent FPGAs overcame DSPs in performance. The number of boards is minimised to 3, consisting of the RF receiver, DSP/FPGA and GPS receiver boards. The design consists of 34 A4 schematic pages (Fig. D.3 (a)), 640 components, 968 nets and 4467 connections. The cost of the required hardware, commercial software, emulators, simulators, programming cables, annual subscription fees etc. is high for the prototype. These concerns lead to a custom FPGA-based design.

5.7 Custom FPGA-Based Design Considerations

DSP, programming and control of the system are simplified by removing the DSP. An FPGA has the resources to perform all the required functionality. The Spartan-2 XC2S200 entered the market in 2001 [191] and has 200,000 equivalent gates. It is replaced by the Spartan-3 XC3S1500 [192], marketed in 2005. The XC3S1500 has 1,500,000 equivalent NAND2 gates. It is based on Virtex-II and Spartan-II technologies at a fraction of a Virtex-II FPGA's cost. The cost of the prototype is significantly reduced.

5.8 Priamos DSP Engine Design

The DSP engine board consists of 7 functional areas, namely DDC, FPGA, SRAM, master oscillator, USB, GPS and FPGA UART interfaces and power supply. The top-level diagram of the 6 – layer PCB is in Fig. D.4. The PCB consists of 323 components, 400 + 14 signal and plane nets, and 476 + 753 signal and plane connections routed. The design consists of 12 A4 circuit schematic pages, numbers 11 - 22 in Fig. D.3 (b).

5.8.1 Digital Down Converter Design

The GC5016 DDC circuit is Fig. D.5. The sampled data on the 40 - pin IDC connector pass through the SN74AVC16244DGGR buffer and connect to DDC AI [15:0] input port. The FPGA controls and programmes the memory mapped GC5016 in a dual-strobe edge-WRMODE using the A [4:0] address bus, C [15:0] data bus, /CE, /RD and /WR pins.

The 32-bits down converted I and Q outputs connect to the FPGA via CD [31:0] bus. ISA commands 1084h and 1085h power-down channels 3 and 4. Programming GC5016 is at RTL level. ISA level command 1080h resets GC5016. 107Ah tri-states CD [31:0] bus. ISA command 1088h disables channel 1 and 2 outputs. RTL commands hold the PFIR coefficients. FirA block is programmed in 1.12 us by issuing 1089h followed by 27 seriatim device specific page - address RAM commands. CicAB block is programmed in 0.44 us by issuing 108Ah followed by 10 seriatim RAM commands. Reset is cleared by issuing 1081h. /SIA is set to high issuing 108Bh. /SO is triggered. CD [31:0] is enabled issuing 1079h.

5.8.2 USB 2.0 Interface Design and Programming

The Cypress CY7C68001 USB 2.0 interface is in Fig. D.6 [199]. Priamos is programmed in Visual C++ 2005, while the computer engineering hardware interfaces are in native C for faster hardware accesses. The dynamically shared priamos2.dll library allows SDR functions for Microsoft Windows and OS/2 operating systems application development. The API allows bi-directional communications between the FPGA and host. 16–bits data is written or read from a register or a set of memory-mapped registers in single or streaming fashion depending on the ISA command. The JTAG daisy-chain is reconfigured through the glueless USB or Ethernet interfaces.

For an address write, data on FD [15:0] are stable at least 3 ns prior the /UFLAGC falling edge. /UFLAGA indicates an address transfer. The active high SLRD indicates a busy interface and queues any transactions. During an address read transaction /UFLAGC is high, /UFLAGA low and the address register is read, while SLRD is high. The data write or read process is similar and /UFLAGB is used instead of /UFLAGA.

5.8.3 FPGA Hardware Design and Configuration

Priamos is built on the XC3S1500-4FG456 FPGA. The 441 connections of the 456-pin BGA device are arranged in 4 A4 pages, as in the FPGA top-level schematic of Fig. D.7. Additional I/O connections to FPGA peripherals are in Fig. D.8. JP1 is a second 40-pin I/O IDC connector initially used for testing. In the final system supports six GC5016 bypassing functions, enables embedded DDC processing and provides the 10/100 Mbps Ethernet interface. The Ethernet interface is in Ch. 7, originally designed for Dimagoras.

Priamos boots by running the host Visual C++ configuration software application. The FPGA programming and special I/O interface allows the system to boot in a variety of methods, as in Fig. D.9. The system supports master serial and JTAG daisy-chain programming, by setting jumpers JP 44 – 46. Unsupervised riometer operation favours master serial programming and independent data logging. The XCF08P-FS48 (U14 in Fig. D.9 and D.12) non-volatile Flash PROM serially transmits 5,214,784 bits to configure the FPGA. JP 31 or 32 bypass the GC5016 (U8 in Fig. D.12) or XCF08P.

JTAG programming was used during all testing phases. During early testing, the 6 – layer Priamos DSP engine prototype of Fig. D.10 and D.11, was programmed using the Xilinx Platform Cable USB, as in Fig. D.12. The coloured flying wires connect to the Xilinx programmer. JP 31 bypasses GC5016.

5.9 Priamos DSP Engine VHDL Design

The FPGA I/Os are in Fig. 5.9. The VHDL code to implement Priamos consists of 42,124 lines. 175 ISA and over 300 SDR commands programme and reconfigure the system. The SDR commands include combinations of ISA commands and parametric parsing. The FPGA design consists of eight mega-functions, namely (from left to right and top to bottom in Fig. D.13): frequency controller, auto-correlator, master controller, digital amplifier, ADC, computer engineering, DDC computer engineering and GPS interfaces.

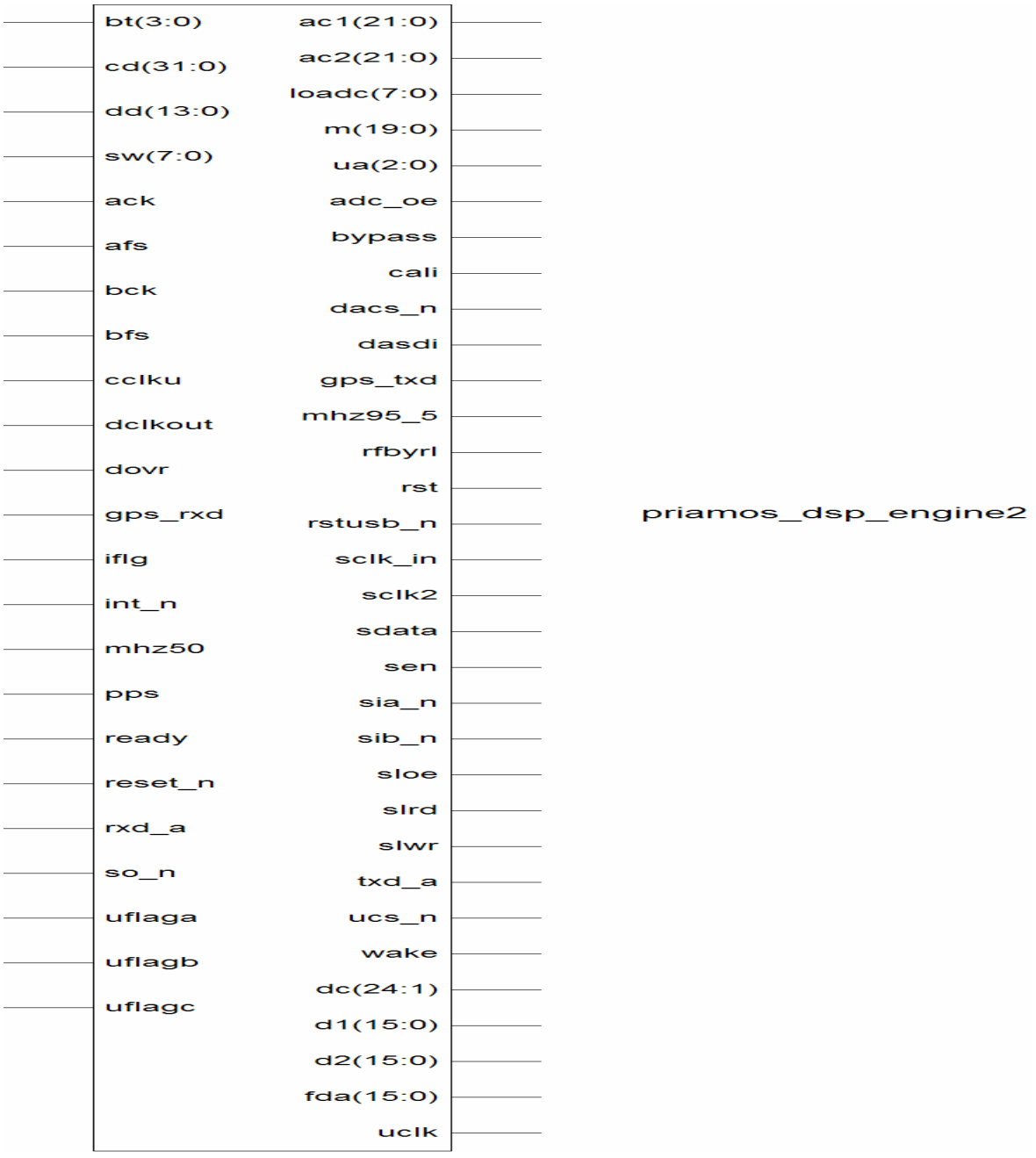


Figure 5.9 Block Diagram for the Priamos DSP Engine.

5.9.1 DDC Computer Engineering Interfaces Design

The top-level block diagram of the ddc_coei mega-function is in Fig. 5.10. ISA 107Dh and 107Eh combined commands, route the GC5016 outputs to the auto-correlator. ISA 107Ch and 107Fh combined operation commands, program GC5016 in bypass mode and route the ADC data via GC5016 to the embedded DDC ddc2 module. ISA 107Ch and 107Dh combined commands route direct ADC data via JP1 to ddc2.

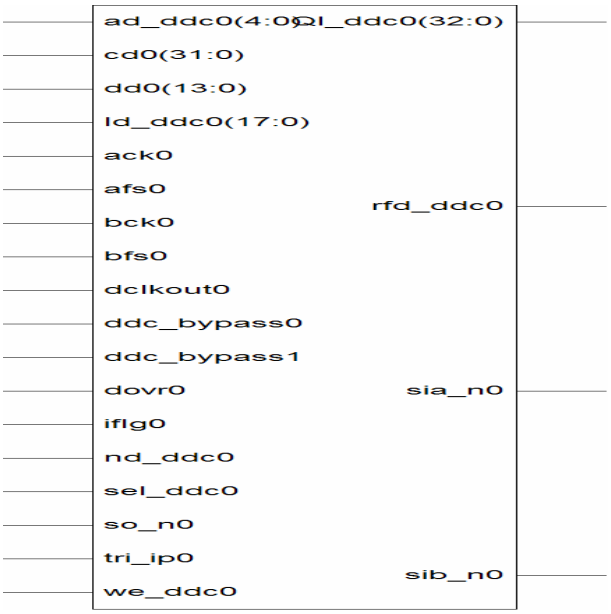


Figure 5.10 Block Diagram for the DDC Interfaces.

The programmable ddc2 module has the same specifications as GC5016. ISA 1041h sets the NCO's 48-bits frequency register to 384B0EBE5319h for a 21 MHz output. ISA 1042h sets the 16-bits phase offset register to 0000h for zero offset. ISA 1043 enables phase dithering for a spur level of -125 dB. The CIC filter [193] decimates by 64 at 95.5 MHz. The CIC gain is 1073741824, compensated by the CIC scale circuit [194]. ISA 1045h sets the coarse gain to 8. The input is 20-bits and output 24. The CIC filter's attenuation at 125 KHz is 0.5 dB in Fig. 5.11, compensated by the FIR filter of the next stage.

The CFIR stage at 1.49 MHz compensates for the 0.5 dB CIC attenuation and decimates by 2. The 21 coefficients are calculated in Matlab and loaded via ld_ddc [17:0]. The sinc factor and power are 0.5 and 5, respectively. The passband, stopband and slope attenuations are 0.01 dB, 39 dB and 59 dB, respectively. The CFIR response is in Fig.

5.12. The combined CIC and CFIR quantised and reference responses up to 0.5 MHz is in Fig. 5.13 and up to 50 MHz in Fig. 5.14.

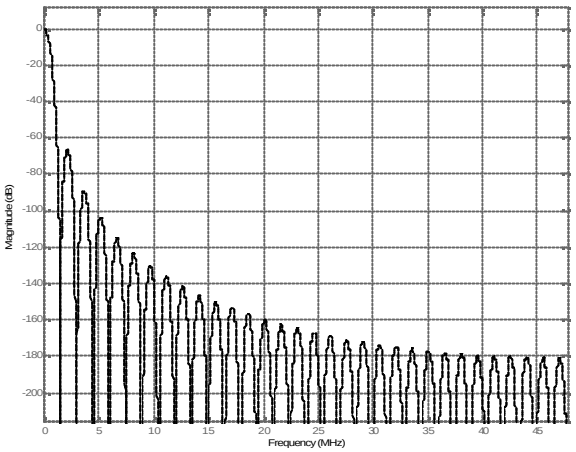


Figure 5.11 CIC Filter's Frequency Response.

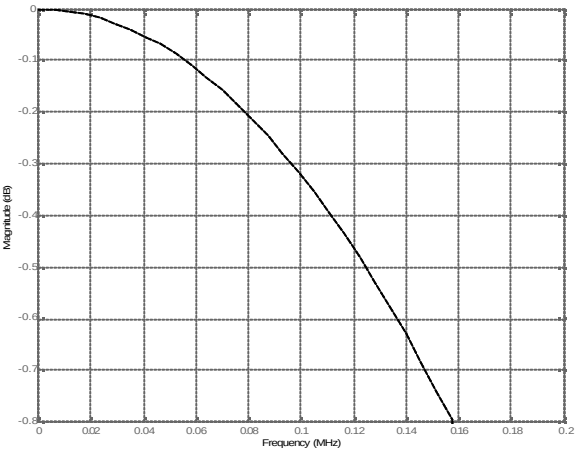


Figure 5.12 CFIR Filter's Frequency Response.

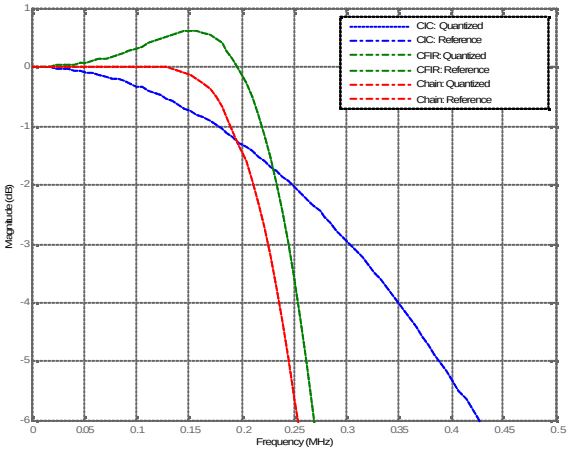


Figure 5.13 CIC, CFIR and Cascaded Output Frequency Response (f < 0.5 MHz).

The 746.093 KHz output passes to the 63 coefficients PFIR filter stage [195]. Its frequency response up to 0.5 MHz is in Fig. 5.15.

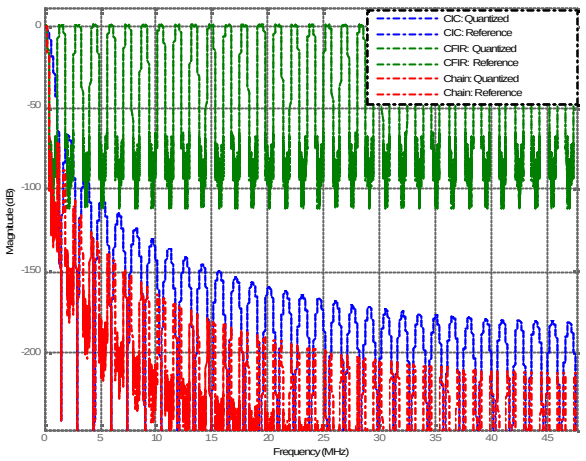


Figure 5.14 CIC, CFIR and Cascaded Output Frequency Response (f < 50 MHz).

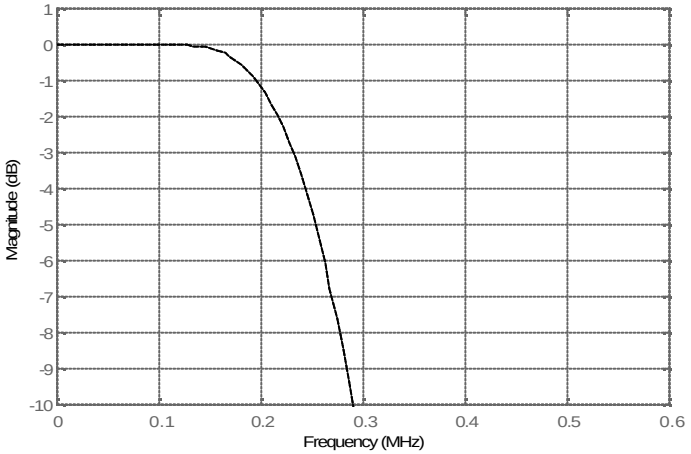


Figure 5.15 PFIR Frequency Response (f < 0.5 MHz).

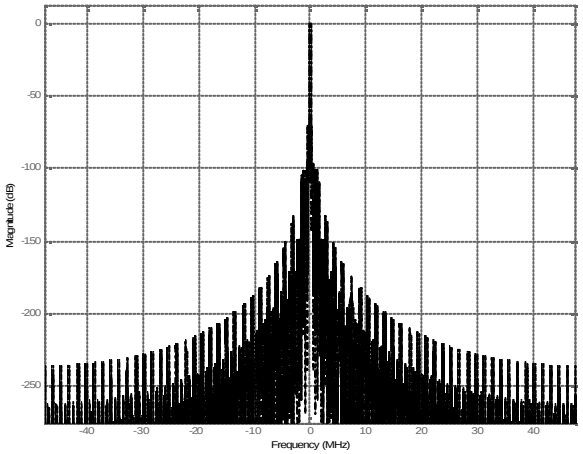


Figure 5.16 Embedded DDC Frequency Response (-50 MHz < f < 50 MHz).

The CIC, CFIR and PFIR cascaded frequency response is in Fig. 5.16 and 5.17 between -50 MHz to 50 MHz and -0.5 MHz to 0.5 MHz, respectively. The peak ripple is 0.0069 dB. The bandwidth is 250 KHz. The output data rate is 373.04 KSPS [196].

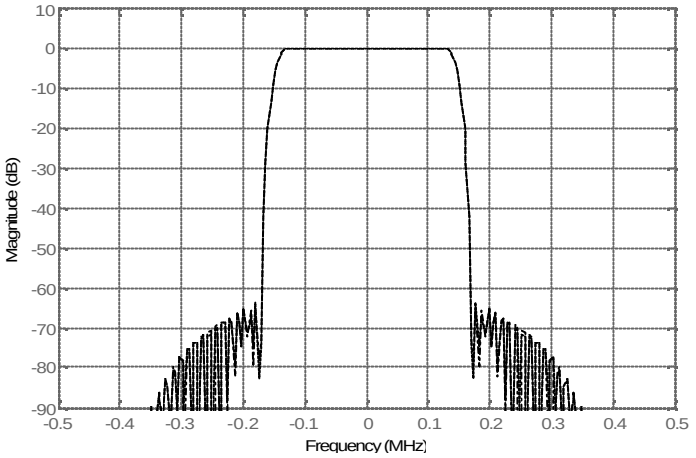


Figure 5.17 Embedded DDC Frequency Response (-0.5 < f < 0.5 MHz).

The system prohibits simultaneous GC5016 and ddc2 operation by issuing a set of mutually exclusive ISA commands. If the GC5016 is active, ISA 1027h powers down ddc2. To activate ddc2, the four-cycle ISA 1025h command is reissued four times, for default functionality, refreshing the global registers. Each 1025h command is followed by a 5-bits address and 18-bits programming data. ISA 1082h and 1083h combined commands power down the remaining GC5016 channels 1 and 2.

Both DDC modules support certain programmable real-time features, such as CIC coarse gain, CIC decimation rate, DDS phase control etc. Reprogramming the DDC modules with new frequency response specifications, for instance bandwidth of 1 MHz, is achieved via reconfiguration and software looping of the configuration files.

5.9.2 Complex Auto-Correlator Design

For auto-correlation I1 = I2 and Q1 = Q2. The complex multiplier's result equals:

$$I = (I_1 I_2 + Q_1 Q_2) = I_1^2 + Q_1^2$$
$$Q = (I_2 Q_1 - I_1 Q_2) = 0 \qquad (5\text{-}12)$$

Where, Q is always zero and I is the power sum of each channel. The implemented auto-correlator receives the ddc_coei 32-bits I and Q data, and clock output from either DDC unit. The two multipliers square the I and Q inputs in Fig. D.14. The results are added and sent to the integrator unit. The integrator sums the 33-bits results for a programmable integration time. When the integration time overlaps trig_int input rises, releasing the 64-bits result to the coei mega-function module of the next section. Trig_int falls and I_xco [63:0] output bus remains constant. At the next cycle the integrator is reset and the process is repeated.

The auto-correlator is by default hardware controlled. Software auto-correlation overrides hardware control and five ISA commands are devised. ISA 1029h, 102Ah and 102Bh commands initialise, activate and halt the auto-correlation, respectively. ISA 102Ch and 102Dh commands trigger and initialise the integrator.

5.9.3 Computer Engineering Interfaces Design

The computer engineering interfaces (coei) module top-level diagram is in Fig. D.15. The coei mega-function receives integrated data via xcor [63:0] bus. Gps_data [31:0] bus carries streaming GPS data. UTC time and geographic position are extracted, updating the 160-bits utc_reg and 224-bits gps_reg public access registers.

Utc_reg structure from MSB to LSB is: GPS ms time of week (32-bits), time accuracy (32-bits), ns of s (32-bits), year (16-bits), month (8-bits), day (8-bits), hour (8-bits), minute (8-bits), seconds (8-bits), valid result (8-bits). Gps_reg structure is: GPS ms time of week (32-bits), longitude (32-bits), latitude (32-bits), height above ellipsoid (32-bits), height above sea (32-bits), horizontal accuracy (32-bits) and vertical accuracy (32-bits).

ISA 10A2h or 10A3h read last valid utc_reg or gps_reg value in 416 ns and 583 ns, respectively. ISA 108Ch enables integrated data timestamping. The timestamped data are routed for an 8 cycle real-time USB or Ethernet transfer or temporarily saved to the 16 Mb SRAM, by ISA 108Eh and 108Fh commands, respectively.

SRAM storage and uclkc referenced retrieval is via address and control busses ac1_c [21:0] and ac2_c [21:0], and data busses d1_c [15:0] and d2_c [15:0]. SRAM is double buffered. By default, ISA 1090h copies the valid contents of utc_reg [63:0] in memory block 1 locations 00000h – 00003h followed by data in 00004h-00007h, repeatedly. Memory buffer 2 operates in the same mode for all commands. For an integration time of 1s, the SRAM holds zero times overlapping values for 36 h. ISA 1091h maximises storage efficiency. Valid UTC time is place in memory locations 00000h – 00003h, followed by data in 00004h-00007h and data only between 00008h-7FFFFh. UTC seriatim values are recovered using 16-bit software counter loops. Non-overlapping values are stored for 72 h.

ISA 10A1h is for software diagnostics. It writes all-1's to SRAM and reads all-3FFFh 1,048,576 times in 87.381 ms. Before reprogramming the storage mode, ISA 10A0h clears all memory locations in 43.69 ms. Other storage modes, in conjunction with 1090h or 1091h commands, are imposed by issuing 1092h or 1093h commands. The data resolution is reduced to 48- or 32-bits and the zero times overlapping values are stored for 108 and 144 h, respectively. In conjunction with the above commands, timed storage and retrieval is devised between 6 h – 72 h in steps of 6 h, by further issuing the ISA 1094h - 109Fh software error controlled commands.

5.9.4 Digital Amplifier and Analogue-to-Digital Converter Interface Designs

The top-level diagram of the digital amplifier interface is in Fig. D.16. Twenty ISA commands are supported by the master controller and transmitted over the SPI interface. ISA level seriatim 1001h - 1014h commands: load RDAC1, load RDAC2, save RDAC1 to EEMEM0, save RDAC2 to EEMEM1, increment RDAC1, decrement RDAC1, increment RDAC2, decrement RDAC2, increment all RDACs, decrement all RDACs, NOP, load EEMEM0 to RDAC1, load EEMEM1 to RDAC2, increment RDAC1 6 dB, decrement RDAC1 6 dB, increment RDAC2 6 dB, decrement RDAC2 6 dB, increment all RDACs 6 dB, decrement all RDACs 6 dB and, finally, reset the digital amplifier, respectively.

The top-level diagram of the ADC interface has the same names as the interface in Fig. 5.35. Twelve ISA commands are supported by the master controller and sent over the modified SPI interface. ISA level seriatim 1015h - 1020h commands: turn DLL on, DLL off, normal operation, all O/Ps 0, all O/Ps 1, power down on, power down off, ADC OE high, ADC OE low, ADC reset on and ADC reset off, respectively.

5.9.5 GPS Interface, Frequency and Master Controller Design

The bi-directional GPS interface of Fig. D.17 routes valid data to the frequency controller of Fig. D.18 and reprograms the ARM7 uP – based GPS receiver. The frequency controller mega-function generates the Priamos timing and synchronisation signals. The global input clock is synchronised with the gps_pps signal to generate the UTC referenced 95.5 MHz on JP1, 50 MHz, 25 MHz, 12.5 MHz, sclk, sclk2, uartclk and clk_integ clock signals.

ISA 102Fh and 1030h commands select either the programmable gps_pps or an internal UTC referenced programmable clock signal as the integration clock (clk_integ), respectively. ISA 103Dh followed by 256 – bits in UBX protocol format reprograms the gps_pps period between 1 ms - 60 s in 32-bits resolution. The time pulse length is set to 10% in 32-bits resolution, to allow more time for combinational processing. Gps_pps is programmed active-high (8-bits). Gps_pps is UTC aligned (8-bits). ISA 102Eh reprograms the internal UTC referenced clock period between 10 ms – 22 min, in 24-bits resolution.

Despite software support, the controller supervises GPS synchronisation. In case of GPS synchronisation loss, if the two signals XOR comparison is 1 for more than 8.04 us, the controller recovers synchronisation by switching to the internal clock. The circuit implements an embedded RTC [197] scheme, based on a custom MC68HC68T1 VHDL implementation, developed for another project. The modified parallel input RTC is UTC compatible and the absolute necessary logic is implemented. The internal UTC register rtc_utc_reg [55:0] is updated every three hours, when GPS is present, via auto-triggering of the 8-bits hour register. The GPS receiver controls utc_reg [159:0] in real-time and when sensing fails, RTC copies rtc_utc_reg to utc_reg [63:8]. FFh is written to utc_reg [7:0] to indicate GPS synchronisation loss. ISA 103Eh updates rtc_utc_reg from GPS. ISA 103Fh copies UTC time from host to rtc_utc_reg.

ISA 1040h senses baud rate. ISA seriatim 1035h – 103Ch commands set the baud rate to: 1200, 2400, 4800, 9600, 19200, 38400, 57600 (default) and 115200 Baud, respectively. ISA 1031h – 1034h reset, coldstart, warmstart (default) and hotstart the GPS receiver.

At the software-level, the devised ISA corresponds to SDR functions parameters. At the hardware-layer, ISA corresponds to machine language instructions. The implemented dual - state machine master controller receives, decodes and executes the current instruction before proceeding to the next instruction. It has 155 I/Os, 267 states and 312 transitions.

5.10 Priamos DSP Engine Unit

The DSP Engine FPGA hardware implementation requires 296,787 equivalent NAND2 gates and runs up to 96 MHz, as presented in Fig. D.19. The fully assembled DSP Engine unit is in Fig. D.20. The top 40-way IDC ribbon cable on the right digitally controls the RF receiver unit. The bottom ribbon cable connects the datapath signals from the receiver to FPGA. Analogue 0 and 15 V, and digital 0 and 5V power supply inputs connect to the back of the unit. Analogue supply is at the top.

The bi-directional communication between the DSP engine and host is achieved via the Ethernet cable on the left. A USB 2.0 and two RS232 ports exist on the left side. The first RS232 port establishes a bi-directional data communication interface between the GPS receiver and DSP engine. The second is spare and can be used as an alternative computer engineering interface to host.

5.11 Conclusion

The possibility of hardware implementing a digital FIR BPF was first investigated. The filter operates at 95.5 MHz sampling frequency, centred at 38.2 MHz and an initial 250 KHz bandwidth. Testing indicated that 9568 coefficients are required. A symmetrical architecture implementation reduces the number of coefficients to 4784. The DSP power required is 913747 MIPS.

The C64x FIR DSP_fir_gen, DSP_fir_r4, DSP_fir_r8 and DSP_fir_sym functions indicated that 478965, 478809, 478416 and 299776 cycles are required to produce the first 200 outputs, respectively. This corresponds to 1500 clock cycles for the DSP_fir_sym function to produce the first output.

The 4784 coefficients filter requires 10091 clock cycles to process the first 16384 FIFO outputs. In this implementation FIFO data are overwritten by new data before getting processed. If the FIFO is paused until the DSP processes 16384 samples of data, a significant amount of streaming data is ignored. If a BPF of fewer coefficients is used, e.g. 48, resulting in a 24^{th} order symmetrical filter, the filter's bandwidth is over 2 MHz. The FIR BPF is not possible to be implemented using any of the available DSP or FPGA devices. A DDC stage is required before the DSP or FPGA, eliminating the BPF's excessive hardware requirements.

The GC5016 DDC device interfaces to TMS320C6416 - 1 GHz DSK via a FIFO module. The prototype consists of 7 boards including the RF Receiver Unit. Due to limited number of I/Os the EMIFA SDRAM interface and most of the programmable features are disabled. The system supports real-time operation only. The GPS receiver connects to host and data timestamping occurs during data logging. An external controller on the HPI bus is still missing to fully control the system. Extra software is needed for data logging and hardware to configure and debug the system.

A custom DSP-based with FPGA co-processor computer architecture is, therefore, considered. Software is in C and assembly language using CCS and in VHDL using Xilinx design flows. Drivers and C/C++ code are needed for data logging. GC5016 is programmed by passing the configuration files through the DSP and via HPI to FPGA.

The XC2S200 FPGA co-processor performs datapath processing sufficiently, but the resources are limited for providing the required flexibility in both hardware and software programming. Taking into account the complexity of the design and prototyping costs, an FPGA-based solution is implemented.

The older XC2S200 FPGA is replaced by the 1.5 million gates XC3S1500 FPGA. The DSP Engine Unit features programmable or reconfigurable control over the FPGA, RF Receiver Unit, dual-DDC processing, external clock generation up to 250 MHz, integration time in the range of 10 ms – 22 min, UTC RTC timekeeping, real-time UTC data timestamped transfer to host and SRAM UTC data timestamped storage up to 144 hours for zero overlapping samples etc. The storage capacity is increased further by using the FPGA's embedded RAM logic.

The USB 2.0 and 10/100 Mbps ports provide a glueless multi-port interface for reading or writing data to the coei mega-function module. More than 300 combined action or parametric parsing SDR commands are devised for real-time programming or reconfiguration, enabling a variety of programming scenarios to be implemented. The DSP Engine Unit is used for fast prototyping of other space physics applications.

Chapter 6 analyses the results of an applied novel design methodology for engineering low-power macroscale optimised fluxgate sensors, for measurements of the complex solar wind – magnetospheric – ionospheric system.

Chapter 6.

Novel Digital Magnetometer for Oracular upper-Atmospheric Studies (DIMAGORAS): System Analysis and Sensor Design

6.1 Introduction

The following two chapters describe the multi-frequency, multi-bandwidth, programmable and reconfigurable Dimagoras system. The chosen architecture is aimed at producing a programmable receiver independent of the fluxgate sensor used. A novel applied design methodology is presented for engineering macroscale optimised sensors measuring complex space physics events. Any ring-core or parallel type fluxgate sensor can be connected to the input, for fast prototyping of different magnetometer instrumentation configurations.

As a fully digital system the sensor's output is sampled after the preamplification stage. The full extent of the complex solar wind – magnetospheric - ionospheric system would be measured by the magnetometer, due to the receiver's programmable DR and integration time. The FPGA implements a reconfigurable filtering scheme, selecting different centre frequencies and signal bandwidths. The system would feature automatic calculation of the Earth's magnetic field, based on the geographic location and automatic comparison between the captured and theoretical magnetic field data for magnetospheric - ionospheric events identification.

The output is in nT and the magnetic field's vector components or total intensity is real-time transferred using UART, USB 2.0 or 10/100 Mbps Ethernet computer engineering ports.

6.2 Background

A digital magnetometer samples the sensor's output after the PA and any analogue filtering stages, eliminating higher-harmonics. The feed-through voltage at the excitation frequency is filtered. False output is measured if the ADC is harmonically distorted.

Phase detection and additional filtering is implemented into the chosen device, as demonstrated using ADSP210200 CPU [63]. The magnetometer exhibits 15 pT rms in the frequency range of 0.03 Hz - 12 Hz. Digital detection has the advantage over switching type variable-width detector that the reference signal is of any shape to match the captured waveform. Oversampling to increase DR is possible, since typical operating frequencies are in the range of 2 - 128 KHz. The input data rates are low and connecting the three channels to an FPGA is feasible. The feedback connection contains a V/I converter eliminating the feedback winding's resistance variation effect.

Based on the analysis of existing and planned magnetometers, it is apparent that magnetometer design is changing rapidly. There are two categories of evolving designs. The first category covers designs where a new sensor is developed and the receiver's architecture is adjusted to the sensor. The second category encompasses designs utilising an existing sensor and improving the receiver's architecture. The reviewed systems are hardwired to a specific function, lacking flexibility in terms of signal processing. The systems are tied to one sensor, operating frequency, bandwidth and DR. There are systems implementing a variable integration time scheme.

For measurements of the Earth's magnetic field, extra functionality is optional. Studying Space Physics events requires flexibility in reconfiguring the instrumentation to perform a new experiment and, if possible, in real-time. Expanding the DR and digitally controlling the analogue circuits, allows Space Physics events to be captured at the edges of the hardwired DR, and beyond, that would otherwise be lost. For hardwired methodologies new hardware is required and time, before a new experiment is attempted. Those designs are still hardwired.

6.3 Dimagoras Specifications and Computer Architecture

The Dimagoras system of Fig. 6.1 features the following:

- Multi-frequency (1 KHz – 1.5 MHz).
- Multi-bandwidth (1 Hz – 4 KHz).
- 16-bit ADC resolution.
- 96 dB DR expandable to 166 dB.
- Noise of 4.7 pT/$\sqrt{\text{Hz}}$ at 1 Hz.
- Long-term drift of 3 pT/day.
- Temperature stability per sensor 0.02 nT/degree.
- Total or component intensity at the output in nT.
- Target axis alignment orthogonality of 0.1 % error.
- Programmable field measurement range of +/- 100 uT.
- Programmable sensitivity of 150 uV/nT maximum value.
- Programmable UTC referenced integration time (10 ms – 22 min). Default is 1 s.
- Reprogrammable GPS functionality.
- Auto-recovery from GPS loss of synchronisation.
- UTC referenced clock management and RTC support.
- Reconfigurable within milliseconds.
- SRAM data storage up to 144 hours or real-time host transfers.
- Multi-port: RS232, USB 2.0 and 10/100 Mbps Fast Ethernet.
- Automatic calculation of the Earth's magnetic field.
- Automatic comparison between the captured and theoretical magnetic field data for events identification.
- Intermagnet and Samnet compatibility.
- Fast prototyping of other Space Physics Instrumentation projects.

6.4 System Analysis

Dimagoras measures the three orthogonal components of the Earth's magnetic field. The tri-axial sensor consists of three novel single-axis fluxgate sensors made of supermalloy. The sensor was imposed to a custom macroscale optimisation technique that significantly reduced the power consumption by a factor of 16.

The programmable sensitivity of the magnetometer is 151 μV/nT to amply cover the +/- 100,000 nT variation range of the Earth's magnetic field. For low-latitude regions, a +/- 60,000 nT range is preferred. The 5 KHz programmable excitation waveform drives the excitation coil to saturation, providing a +/- 60 mA peak-to-peak current.

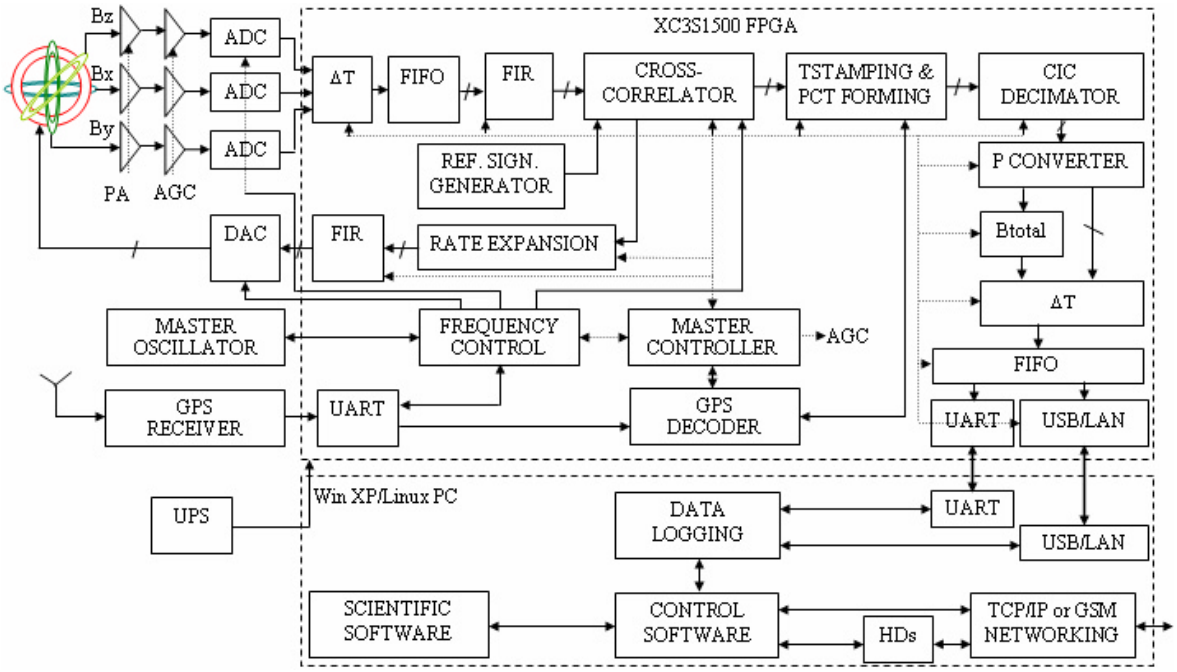


Figure 6.1 Dimagoras Computer Architecture.

The PA and digital amplifier, amplify each sensor's output by 20 dB. Both amplifiers provide LF filtering to minimise noise. The master controller controls the AGC interface. Three 16-bits AD7621 ADCs sample the three signals. The ADC accepts a differential voltage input of +/- 2.5 V. 16 bits provide maximum 96 dB of dynamic range. The AGC is employed when specific thresholds are exceeded, increasing gain resolution up to 166 dB.

Testing ensures that large amplification is not increasing noise. Fluxgate sensors tuned in the range 1 KHz – 1.5 MHz are sampled. Existing sensors are tuned between 8 KHz – 100 KHz. The ADC samples at 0.9 MHz for a sensor tuned at 100 KHz. Exceeding oversampling increases the internal noise.

The digital FIR filter, selects the second harmonic output. All odd harmonics are nullified by the core. The upper LPF cut-off frequency is 15 KHz. The reconfigurable bandwidth is in the range 1 Hz – 4 KHz. The system's default bandwidth is 10 Hz, increasing the filter's complexity, compared to a 4 KHz single-stage filter. For a bandwidth of 10 Hz, three CIC filters are used.

The traditional analogue PSD is digitally implemented with improved performance. A reference waveform is generated digitally, recreating the sensor's output and multiplied with the FIR filter's output. The reference waveform resembles the analogue PSD switch on and off pulse. However, the 1-bit resolution is replaced by 16-bits resolution.

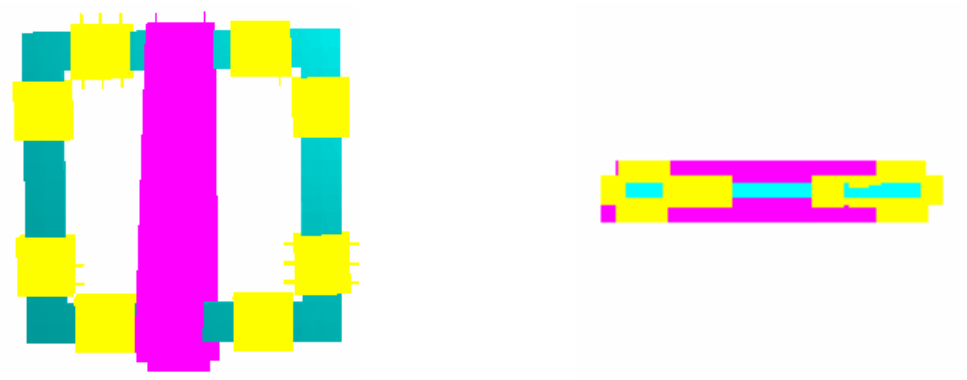
The programmable GPS receiver interface provides UTC time and geographical position information. The cross-correlator's programmable UTC referenced integration time is between 10 ms – 22 min. The outputs of the three integrators are UTC timestamped. The CIC decimator stages provide the required bandwidth.

The interpolator and FIR filter at the feedback loop reduce the DAC's quantisation noise. FIR LPF filtering restricts the noise to system's bandwidth. The decimator provides a relative power measurement. An internal calibration routine assigns a relative power measurement to a known magnetic field value. The intensity values are real-time transferred over the selected UART, USB 2.0 or 10/100 Mbps Ethernet interface or temporarily stored into SRAM for up to 144 h.

6.5 Single-Axis Sensor Design

Several fluxgate sensors of the race-track and ring-core types have been designed and simulated using the Finite Integration Theory (FIT) method. FIT is associated with the Finite Difference Time Domain (FDTD) method. However, FIT contains in the time domain both static and the frequency domain.

The basic simulation model of Fig. 6.2 consists of an excitation coil of 240 turns and a sensor coil of 50 turns. The dimensions of the core are 2 cm x 2 cm x 0.2 cm. The aim is to create an optimised sensor that saturates at a current much smaller (<100mA) than the values quoted in the papers reviewed ($\approx$1 A) [201-202], to reduce power consumption by a factor of sixteen. Low power consumption has only been seen on MEMS sensors [203], after optimisation of the structure, usually by following a trial-by-error procedure. The initial design is a combination of a race-track of eight layers etched from a sheet of amorphous magnetic material [204] embedded in the shape of a standard MEMS square fluxgate sensor [205]. The new design is inheriting the advantages of both technologies.



(a) (b)

Figure 6.2 (a) xy, (b) yz, Projections of the Basic Race-Track Fluxgate Sensor.

The square frame does not improve the electromagnetic performance and an extensive optimisation procedure is required. A rectangle with an aspect ratio of length (x) / width (y) $\approx$ 3 and the sensor coiled around the middle of the two x branches can be used for single-axis measurements. The y-axis of Fig. 6.2 could accommodate a second sensor coil for the y-dimension.

Different soft [206-207] and hard magnetic materials [206-208] have been considered for modelling the core and a list of suitable soft magnetic materials is in Table 6-1. Hard magnetic materials exhibit a wide B (H) curve and were eliminated from the selection process.

Material and composition	μ_i	μ_{max}	H_c (A/m)	B_{sat} (T)	ρ ($\mu\Omega$ cm)
Iron (99.6% Fe)	300	5,000	80	2.1	14
Silicon-iron, grain orientated, cold reduced (3.2% Si, 96.8% Fe)	2,000	70,000	8	2.0	48
Rhometal (36% Ni, 64% Fe)	1,800	7,000	12	0.9	85
Supermalloy (79% Ni, 15% Fe, 5% Mo, 1% Mn)	100,000	1,000,000	0.2	0.8	65
Permendur (49% Fe, 49% Co, 2% V)	800	5,000	180	2.4	28

Table 6-1. Soft Magnetic Alloys.

The chosen material would have a high as possible maximum permeability μ_{max} and a low as possible saturation flux density B_{sat}. The supermalloy was chosen for this study. The B (H) curve is in Fig. 6.3. Supermalloy has a steep slope in the easy magnetisation region and a reasonable flat slope in the hard magnetisation region towards magnetic saturation.

The response is obtained by applying an external field of 1 T in the x direction, as in Fig. 6.4. The sensor is rotated around its axis to measure its directionality. During 3-D transient analysis, a 5 KHz square wave of +/- 250mA was injected to the excitation coil. The voltage is measured at the sensor coil's output.

At instance 0, when no current is applied to the excitation coil the structure absorbs the incoming wave, as in Fig. 6.5.

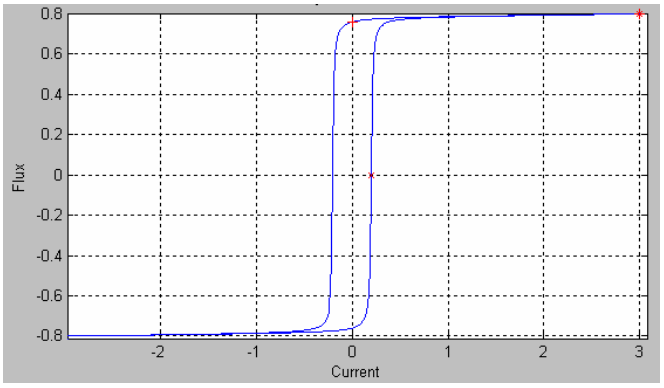


Figure 6.3 Supermalloy Magnetisation B(H) Curve (T(A/m)).

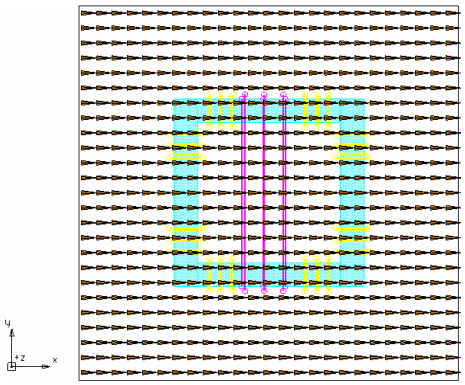
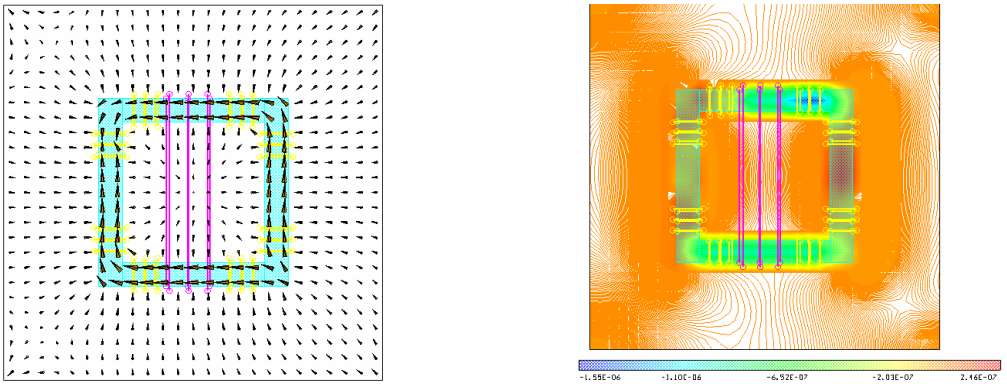


Figure 6.4 X-Axis External Vector Field (1 T).

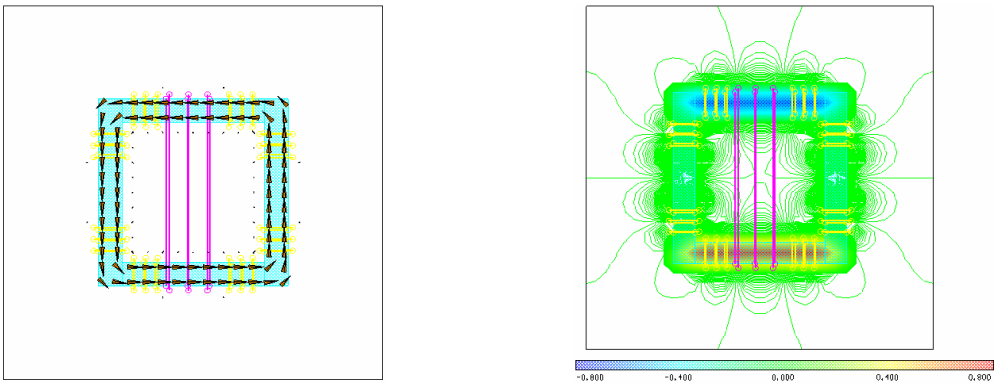


(a) (b)

Figure 6.5 (a) Arrow and (b) Contour Diagrams of B (Iexc = 0).

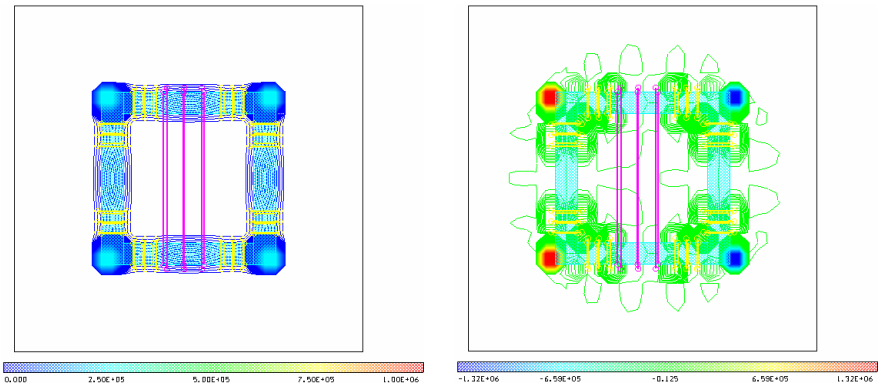
The results for the maximum excitation current value are in Fig. 6.6 (a) and (b), using arrow and a contour diagrams.

At saturation the low-y and high-y branches of the core resume the B_{sat} value of 0.8 T. B outside the core is 0, since all magnetic lines are repressed. The permeability distribution at saturation is in Fig. 6.7 (a).



(a) (b)

Figure 6.6 (a) Arrow and (b) Contour Diagrams of B at Magnetic Saturation.



(a) (b)

Figure 6.7 (a) Permeability Distribution at Magnetic Saturation, (b) Maxwell Stress and Lorentz Force Distribution.

The force F (Fx, Fy and Fz) and torque M on the z-axis (Mz) results for the different materials are in Table 6-2 and in Fig. 6.7 (b). The force is calculated using the Maxwell's stress tensor and Lorentz force for the excitation coil and sensor's winding. The Maxwell's stress tensor calculates the surface integral of the material area, where the force under study is applied. Flux density and field strength allocated on the grid or dual grid are required for high accuracy results. The hot red and blue areas near the corners are areas not taken into account in the calculation of the integral. The validity of the results is not affected and it is overcome for circular/torus shaped cores.

During the transient response analysis the electric field strength, magnetic flux density, eddy currents and relative permeability have all been monitored.

Method	Material	Fx	Fy	Fz	Mz
Maxwell-stress	Space	0	0	0	0
Maxwell-stress	Core	-0.3e-6	-0.12e-8	-0.33e-8	-0.8e-8
Lorentz	Excitation & Sensor Coils	0.96e-9	0.3e-9	0.7e-10	0.9e-11

Table 6-2. Maxwell Stress and Lorentz Force Results.

Based on these measurements the voltage or electromotive force (EMF) is calculated using the Faraday's law [209] by eq. (6-1):

$$V = \oint EdL = -\iint \frac{\partial B}{\partial t} ds \qquad (6\text{-}1)$$

where, $\oint EdL$ is the line integral around the sensor coil,

$\iint \frac{\partial B}{\partial t} ds$ is the surface integral of $\frac{\partial B}{\partial t}$ over the sensor coil.

The raw voltage output depends on all the parameters taken into account in the above simulations and it contains harmonics of the excitation field. A monotonic excitation field is given by eq. (6-2):

$$H = H_{max} \sin(\omega t) \qquad (6\text{-}2)$$

The symmetrical B(H) characteristic curve used to model the nonlinearity of the supermalloy core is by definition a third order polynomial, written as:

$$B(H) = a_1 H - a_3 H^3 \qquad (6\text{-}3)$$

From the arrow plots of Fig. 6.5 (a) and Fig. 6.6 (a) it is obvious that no matter whether the core is at the zero crossing of the initial magnetisation curve or at the end of the hard magnetisation region towards saturation, respectively, there subsists an internal strictly oriented circulating field. In the former figure due to the external field only, while in the latter due to the excitation field only. Within the linear magnetisation region this field is a concoction of both and seizes the form of eq. (6-4):

$$H_{core} = H_{space} + H \qquad (6\text{-}4)$$

Stepping into Faraday's law: $$V = -NA\frac{\partial B}{\partial t} \qquad (6\text{-}5)$$

Normalising the output voltage and solving:

$$\begin{aligned} V_n &= -\frac{V}{NA} = B_{max}\omega(a_1 H_{max} - 3a_3 H_{max} H_{space}^2 - \frac{3}{4}a_3 H_{max}^3)\cos(\omega t) \\ &+ 3B_{max}\omega a_3 H_{space} H_{max}^2 \sin(2\omega t) + \frac{3}{4}B_{max}\omega a_3 H_{max}^2 \cos(3\omega t) \end{aligned} \qquad (6\text{-}6)$$

The product containing the $\sin(2\omega t)$ factor is the second harmonic output:

$$V_2 = 3B_{max}\omega a_3 H_{space} H_{max}^2 \sin(2\omega t) = \psi \sin(2\omega t) \qquad (6\text{-}7)$$

where, $\psi = 3B_{max}\omega a_3 H_{space} H_{max}^2$

The output voltage is a function of the external field, excitation field, excitation frequency, core size and the characteristic curve of the material. In parallel type cores the second harmonic is derived using magnetic filtering, which involves matching two identical linear probes measuring the field difference between two points. Matching is avoided using the presented structure. In parallel type sensors BPFs distinguish the 2nd from the 1st and 3rd harmonics. The presented structure nullifies all odd harmonics without magnetic filtering and a LPF at the 3rd (15 KHz) harmonic extracts the 2nd harmonic. A Matlab Simulink model processes the sensor's output in Fig. 6.8.

A 15th order FIR butterworth LPF with cut-off frequency at the 3rd harmonic (15 KHz) is sampling at 100 KHz. Its frequency response is in Fig. 6.9.

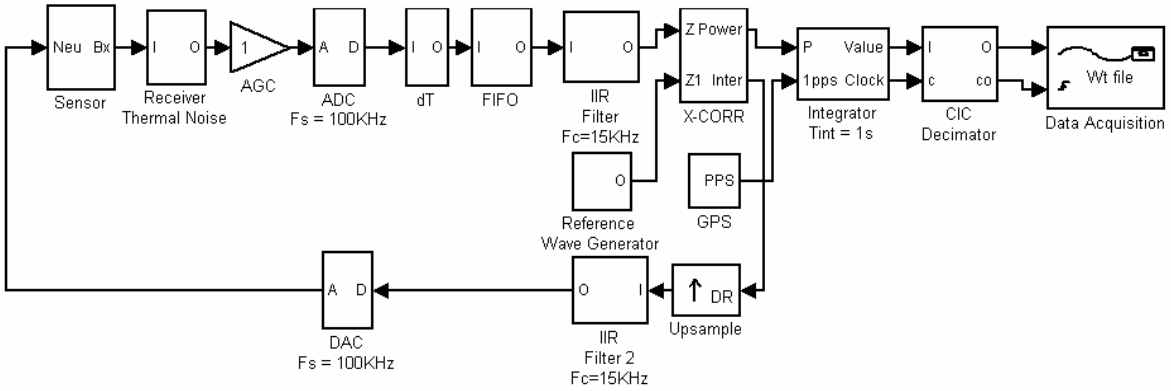


Figure 6.8 Dimagoras Matlab Simulink Model.

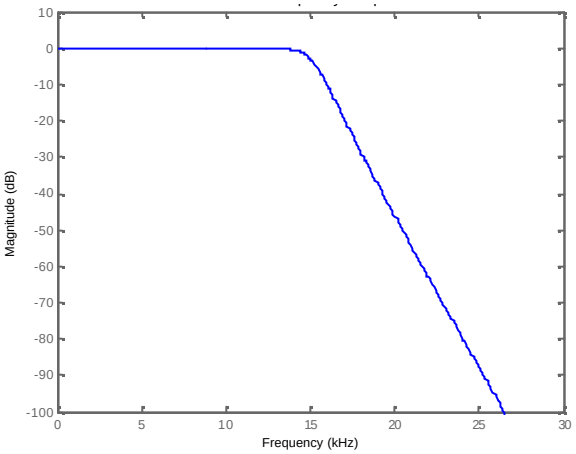


Figure 6.9 FIR LPF Filter Frequency Response.

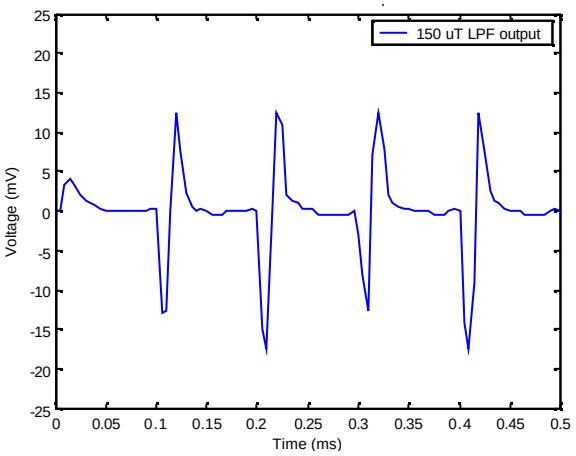


Figure 6.10 Sensor's Output Response for B = 150 uT.

The sensor output for a 150 uT external field is in Fig. 6.10. Vpp is 29.6 mV.

The simulations were repeated for external field values between 0 and 300 uT and the results are in Fig. 6.11.

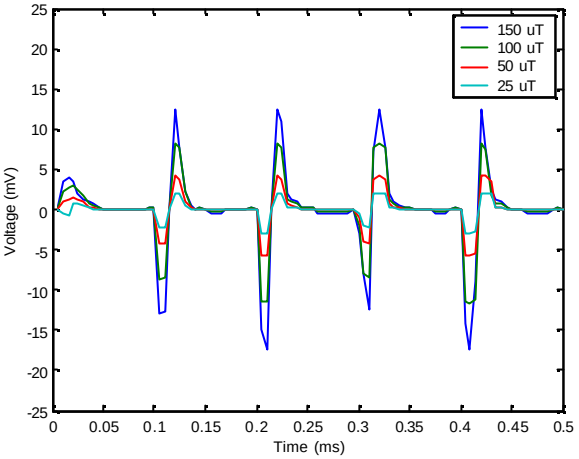


Figure 6.11 Sensor's Output Response for B = 25, 50, 100 and 150 uT.

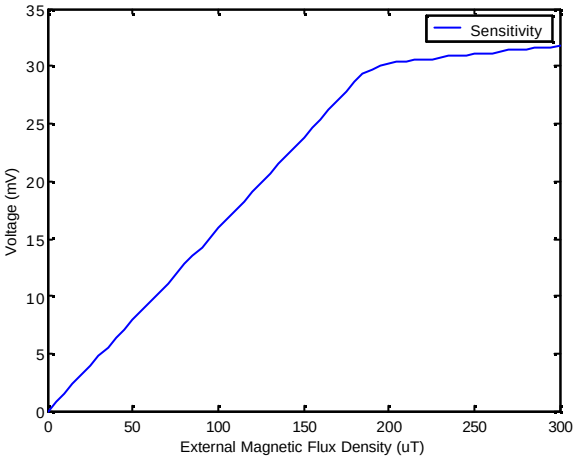


Figure 6.12 Sensor's Sensitivity Diagram.

The Vpp results of all the simulations are plotted in Fig. 6.12 to portray the sensor's sensitivity. The measured sensitivity is 189 uV/nT.

6.6 Single-Axis Sensor Optimisation

At the zero-crossing of the B (H) curve the external field is attracted by the core in Fig. 6.13 (a) and flows through the core due to its weak reluctance in Fig. 6.13 (b). The opposite occurs at saturation. In Fig. 6.13 (b), the magnetic field is entering the structure from branch 1, is split between branches 2 and 3 and exits the structure through branch 4.

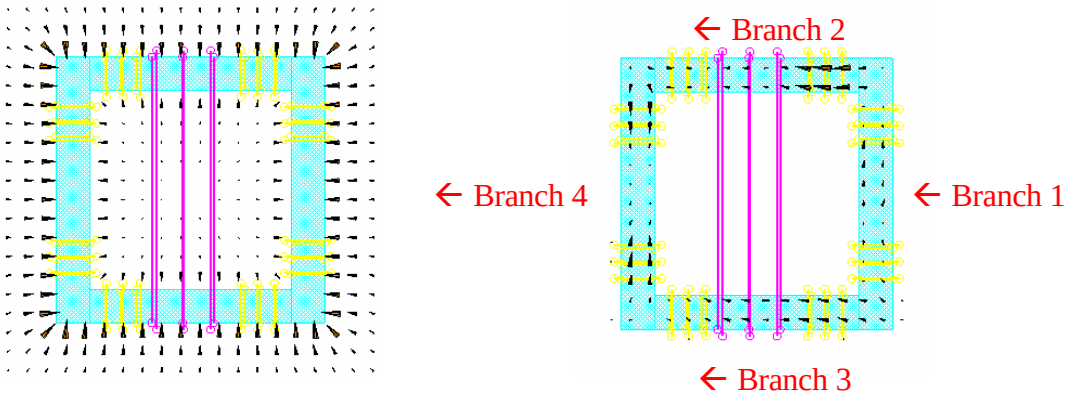


Figure 6.13 (a) External Field (b) External Field Flow Through the Core at Premagnetisation.

The opposition to magnetic flux in any branch of the core is called reluctance $\Re$ [210]:

$$\Re = \frac{l}{A\mu_o\mu_r} \qquad (6\text{-}8)$$

where, $\Re$ is the reluctance (A-turns/Wb), l the length (m), μ_o the permeability of free space, μ_r the relative permeability (H/m) and A is the cross-sectional area of the magnetic circuit (m^2).

Consider the structure of Fig. 6.14 (a) and its magnetic model in Fig. 6.14 (b). Reluctance in magnetism is represented by resistance in electrism. The flux through R1, R4-6 and R9-10 is the same since they are in series.

The flux through R2 and R3 equals to:

$$\Phi_2 = \Phi_3 \frac{R_3}{R_1 + R_2} \quad \text{and} \quad \Phi_3 = \Phi_2 \frac{R_2}{R_1 + R_2} \tag{6-9}$$

$$\frac{\Phi_3}{\Phi_2} = \frac{R_2}{R_3} = \mu_r \frac{A_3}{A_2} = 10^6 \Rightarrow \Phi_3 >> \Phi_2 \tag{6-10}$$

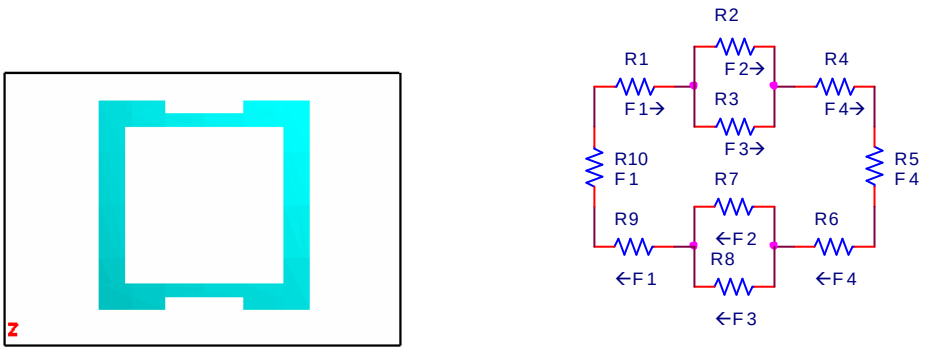
The relative permeability is the maximum permeability in electromagnetics, 10^6. The area ratio equals to 1. Therefore, the air gap fringing flux is negligible.

$$\Phi_1 \equiv \Phi_3 \equiv \Phi_4 \Rightarrow B_1 A_1 = B_3 A_3 = B_4 A_4 \tag{6-11}$$

For $A_1 / A_3 = P$,

$$B_3 = P B_1 \tag{6-12}$$

Therefore, the magnetic flux density through R3 and R7 is P times higher than the flux flowing through the rest of the magnetic circuit.



(a) (b)

Figure 6.14 (a) Modified Core (b) Flux Flow Through the Modified Core.

From equations (6-13) and (6-14) [210] an expression is obtained relating B and the excitation current:

$$L = \frac{N\Phi}{I_{exc}} \Rightarrow \Phi = \frac{I_{exc} L}{N} \tag{6-13}$$

$$B = \frac{\Phi}{A} \Rightarrow \Phi = BA \tag{6-14}$$

$$BA = \frac{IL}{N} \Rightarrow B = I_{exc} \frac{L}{AN} \Rightarrow B \propto I_{exc} \tag{6-15}$$

From eq. (6-12) and (6-15) a relation for the saturation currents is obtained:

$$I_{sat3} = \frac{I_{sat1}}{P} = \frac{I_{sat1}}{4} \approx 60mA \qquad (6\text{-}16)$$

The field flowing through the structure is not the same as the field applied to the material. The magnetisation effect creates free poles at the edges of the structure. These poles in turn create an opposing field to the one applied. This effect is called demagnetisation [211]. The field inside the core equals:

$$H_{core} = \frac{H_{ext}}{1 + N_d \mu_r} \qquad (6\text{-}17)$$

where, H_{core} is the internal field, H_{ext} is the external field, N_d is the demagnetisation factor and μ_r the relative permeability of the supermalloy.

A ferromagnetic ellipsoid is the only shape, which has the same magnetisation and demagnetisation fields throughout its structure. Using Cartesian coordinates N_d is diagonalised and the corresponding demagnetising factors for the xyz coordinates are combined by eq. (6-18):

$$N_x + N_y + N_z = 1 \qquad (6\text{-}18)$$

For a sphere: $$N_x = N_y = N_z = 1/3 \qquad (6\text{-}19)$$

For the simulated sensor of the previous section:

$$N_z = 1, N_x = N_y = 0 \qquad (6\text{-}20)$$

For sensors of the parallel type core, assuming the rod is placed on the y-axis:

$$N_y = 0, N_x = N_z = 0.5 \qquad (6\text{-}21)$$

In general, N_d decreases as the length versus cross-sectional area A ratio increases. In order to find the optimum sensor design several cores have been simulated and the magnetic flux through the core has been measured using the newly calculated excitation current value given by eq. (6-16). Figure 6.15 shows the results from the previously simulated supermalloy sensor at the x-direction, which saturates at 0.8 T for an excitation current of 250 mA.

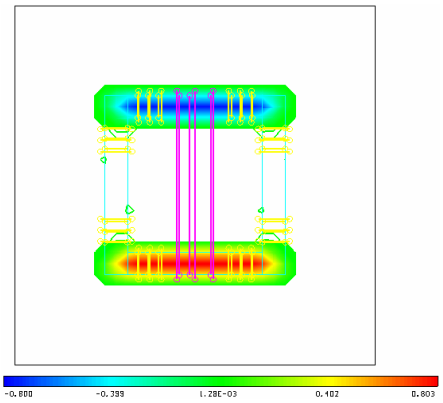


Figure 6.15 Supermalloy Core at Saturation (B = 0.8 T, Iexc = 250 mA).

The excitation current was reduced to 60 mA and B in the x-axis is 0.3 T. The core is not at saturation.

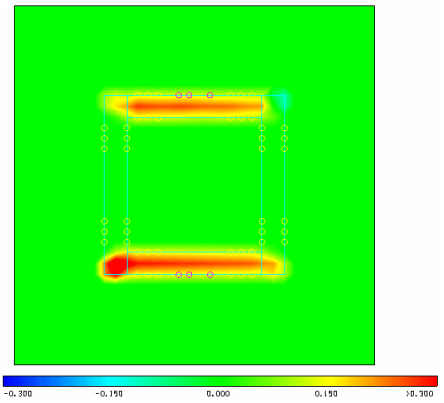
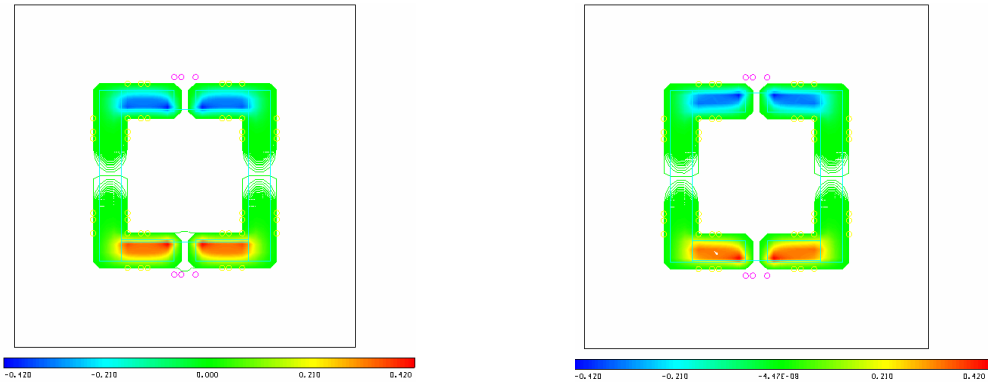


Figure 6.16 Magnetic Flux Density Distribution (B = 0.3 T, Iexc = 60 mA).

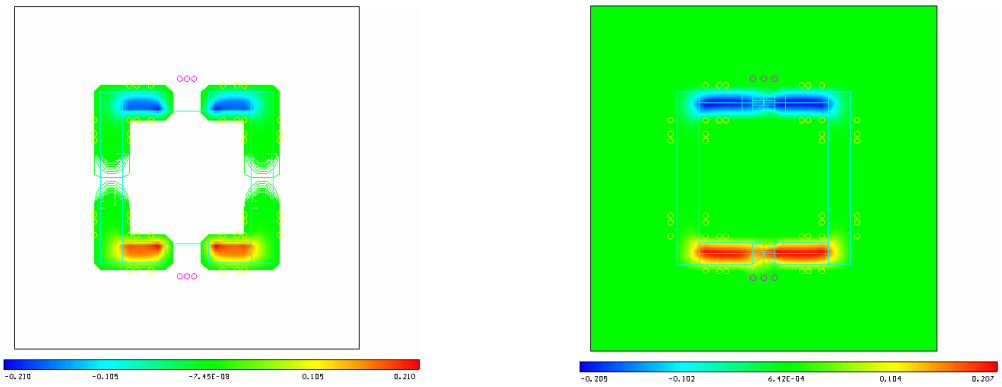
A link of 2.5 mm length (l) and 1 mm width (w) was added corresponding to R3 of Fig. 6.14. For the same excitation current of 60 mA, B equals to 0.42 T, as in Fig. 6.17 (a). The core is not at saturation. The same link was added in place of R2 of Fig. 6.14. The results of Fig. 6.17 (b) match the results of Fig. 6.17 (a).

In Fig. 6.18 (a) the link's l is doubled to 5 mm and B is halved to 0.21 T. In Fig. 6.18 (b) the link is replaced by two facing cones with a total l of 3 mm and no space in between (B = 0.207 T). In Fig. 6.19 (a) a link of l = 5 mm and w = 1 mm between two cones of l=1.5 mm (total l = 8 mm)(B=0.4T). In Fig. 6.19 (b) the link's l = 2.5 mm and the cone's 1.5 mm (B=0.68T). Fig. 6.20 shows the structure for link's l = 2 mm, cone's l = 2 mm (Bsat=0.8T).



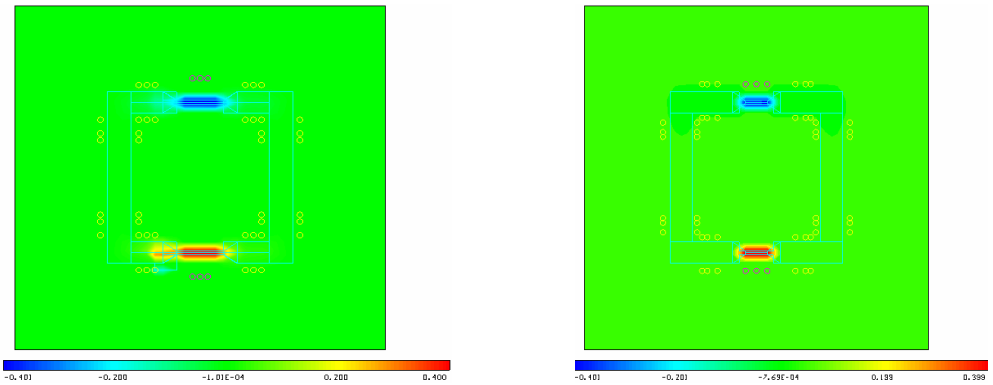
(a) (b)

Figure 6.17 Magnetic Flux Density Distribution (B = 0.42 T, Iexc = 60 mA).



(a) (b)

Figure 6.18 (a) B = 0.21 T, Iexc = 60 mA (b) B = 0.207 T, Iexc = 60 mA.



(a) (b)

Figure 6.19 (a) B = 0.4 T, Iexc = 60 mA (b) B = 0.68 T, Iexc = 60 mA.

After a trial-by-error procedure the optimum core structure is determined. The sensor is tested for a varying external field and the results for the bottom x-branch, of Fig. 6.20, are in Fig. 6.21. The link has sensitivity of 197 uV/nT. The B field at 25, 50 and 100 uT is plotted. Vpp is measured to be 19.45 mV for an external B of 100 uT.

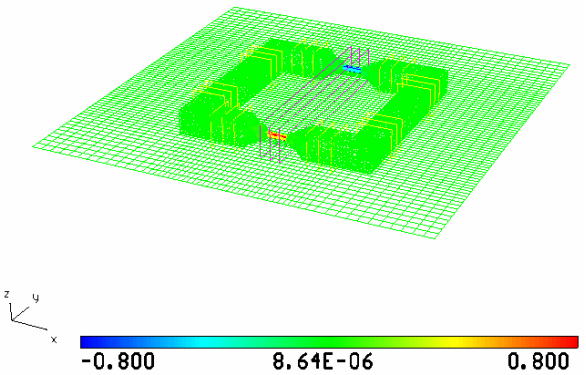


Figure 6.20 B Distribution (Bsat = 0.8 T, Iexc = 60 mA).

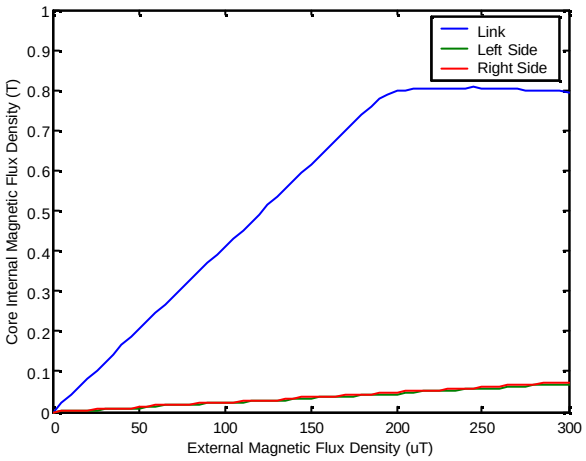


Figure 6.21 Optimised Sensor's Sensitivity Diagram for Bottom x-Branch.

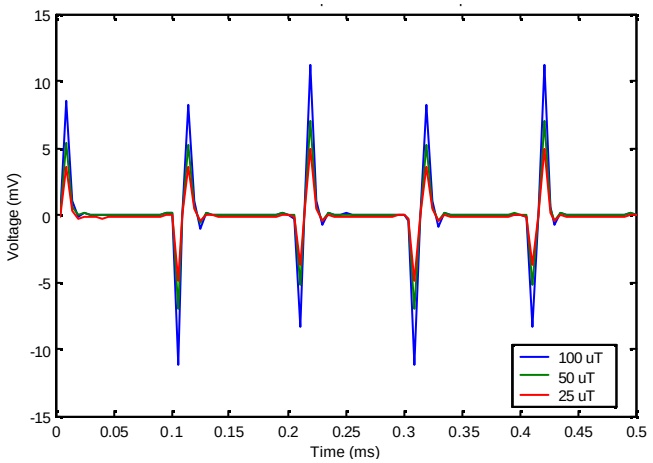


Figure 6.22 Sensor's Output Response for B = 25, 50 and 100 uT.

The sensitivity of the optimised sensor is in Fig. 6.23. The sensor has sensitivity of 151 uV/nT. The response for fields of 250 and 300 uT is in Fig. 6.24.

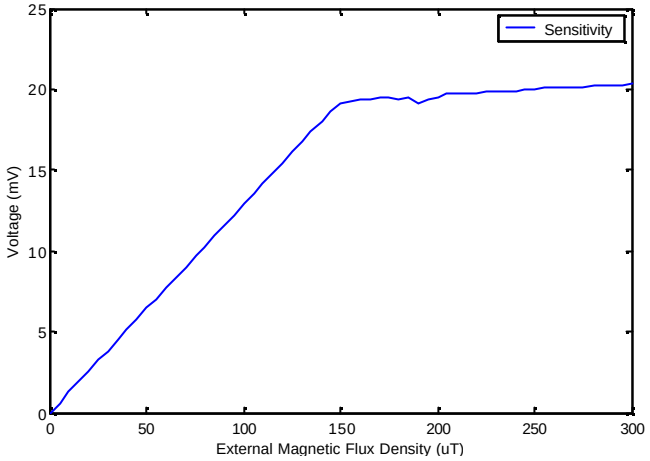


Figure 6.23 Optimised Sensor's Sensitivity Diagram.

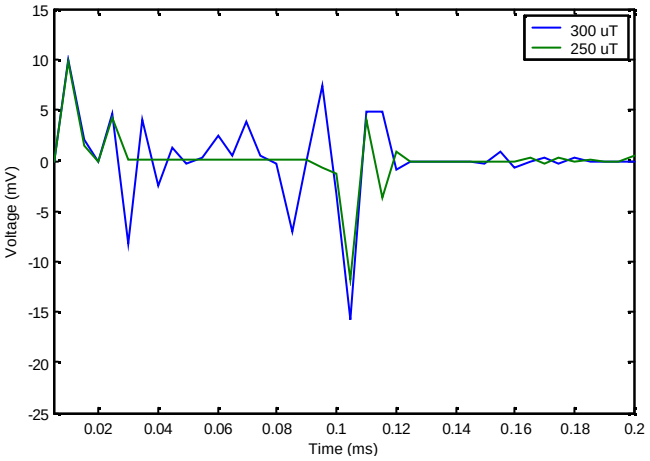


Figure 6.24 Sensor's Output Response for B = 250 and 300 uT.

The design of the optimised version of the single-axis sensor is completed. The sensor is saturated by an excitation current of 60 mA, four times less the initial specifications of 250 mA. The power consumption is reduced by a factor of 16. The sensor has a guaranteed sensitivity of 100 uV/nT and a Vpp output of 19.45 mV to amply cover the Earth's magnetic field variation. The sensor has maximum sensitivity of 151 uV/nT.

6.7 Dual-Axis Sensor Design

The optimisation technique is applied to design a dual-axis sensor. The y-branches accommodate the conical-link structure and a y-axis coil, in Fig. 6.25. The core saturates at 0.4 T for Iexc = 60 mA.

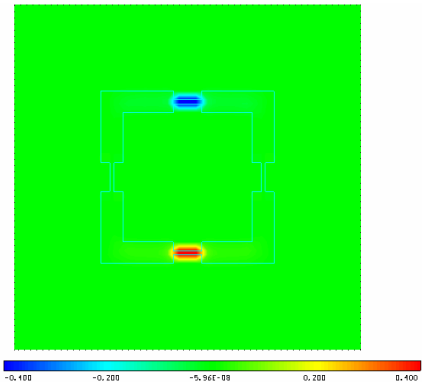
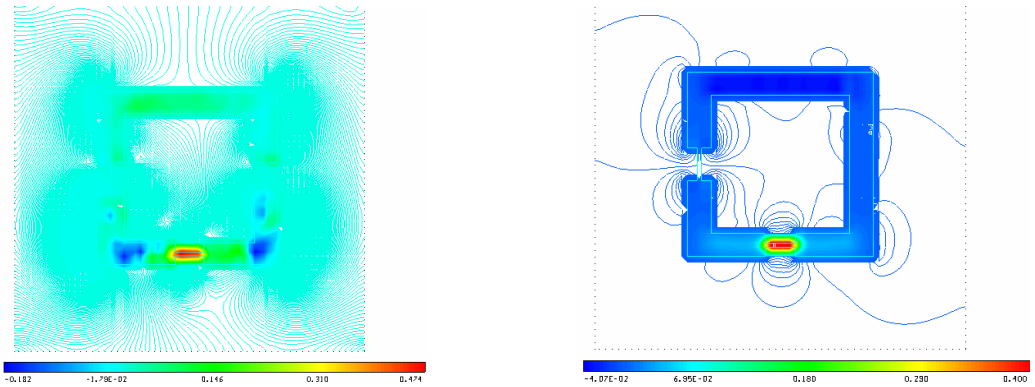


Figure 6.25 X-Axis Magnetic Flux Density Distribution (B = 0.4 T, Iexc = 60 mA).



(a) (b)

Figure 6.26 Magnetic Flux Density Distribution (a) Bsat = 0.474 T (b) B = 0.408 T.

The core was imposed to modifications (e.g. link's l = 1, 2, 4 or 8 mm, cone's l = 1, 3, 5 or 8 mm). The results are similar to Fig. 6.25. Reaching saturation is not possible.

The top cone-link structure is removed (Bsat = 0.474 T), in Fig. 6.26 (a). The right cone-link is additionally removed (Bsat = 0.408 T), in Fig. 6.26 (b). The number of the excitation coil's turns is increased from 24 to 32 (Bsat = 0.468 T), in Fig. 6.27. Iexc is modified next. After extensively testing the core, the results are in Fig. 6.28.

For an excitation coil of 32 turns, Iexc equals 1.4 mA. The core modifications and the 32 turns of the excitation coil, saturate the core at 0.8 T for Iexc = 1.4 mA. This corresponds to a power reduction by a factor of 42. Compared to the optimised sensor, it signifies an immense power reduction by a factor of 1764.

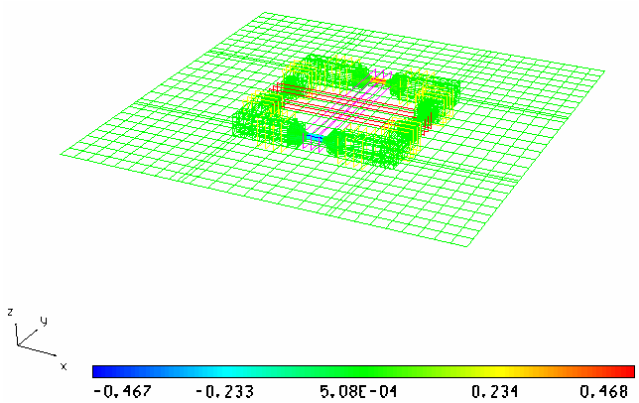
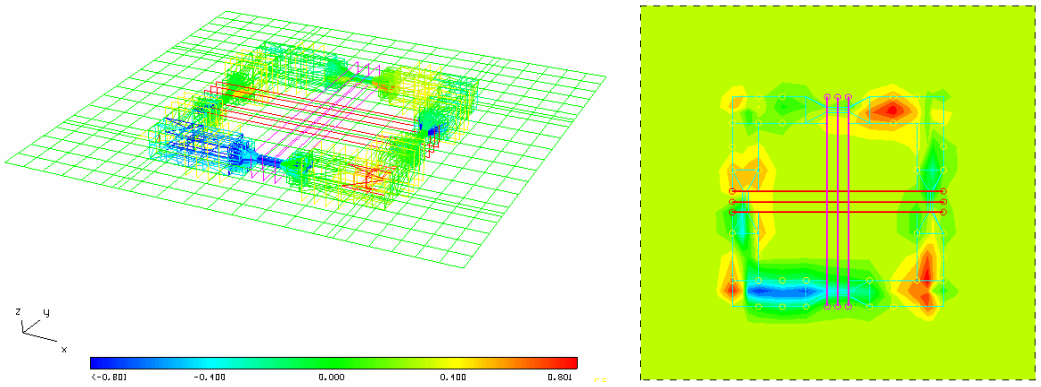


Figure 6.27 Magnetic Flux Density Distribution (Bsat = 0.468 T).



(a) (b)

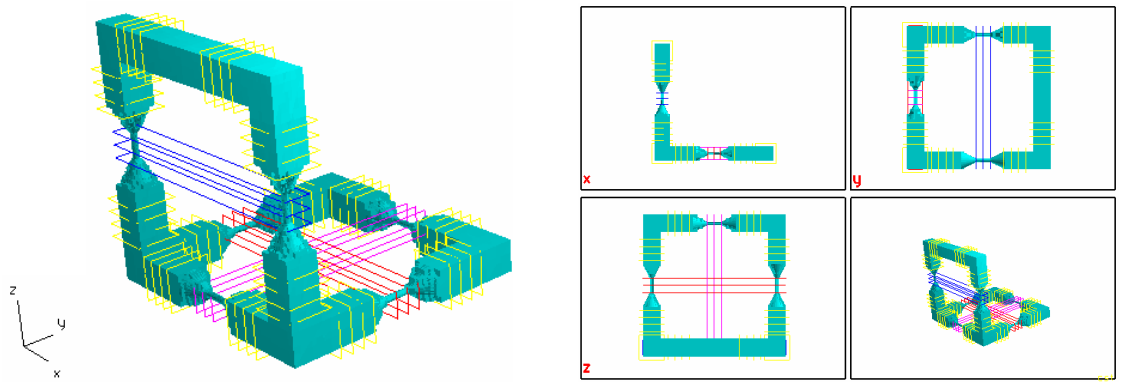
Figure 6.28 Magnetic Flux Density Distribution (Bsat = 0.8 T, Iexc = 1.4 mA). (a) 3-Dimensional Model (b) z-Cut Cross-Section.

The sensor's sensitivity is 49 uV/nT. It corresponds to a reduction by a factor of 3. Non-linear effects were also generated, in Fig. 6.28. Although the core saturates negatively in the y-axis centre, demagnetisation effects heavily saturate the corners.

The solution was to split the different dimension measurement sensors to different planes and to implement the optimisation technique to an intermediate composite dimension. The magnetic paths should be equal to each other to minimise non-linear and demagnetisation effects. The next section applies this approach into the design of a compact 3-D sensor.

6.8 Three-Axis Sensor Design and Optimisation

An expansion of the dual-axis sensor is in Fig. 6.29 and 6.30. The excitation coil has 56 turns. The core saturates at 0.8 T for Iexc = 35 uA. The sensitivity is 70 uV/nT.



(a) (b)

Figure 6.29 Basic 3-Dimensional Sensor (a) 3-D Model (b) XYZ Projections.

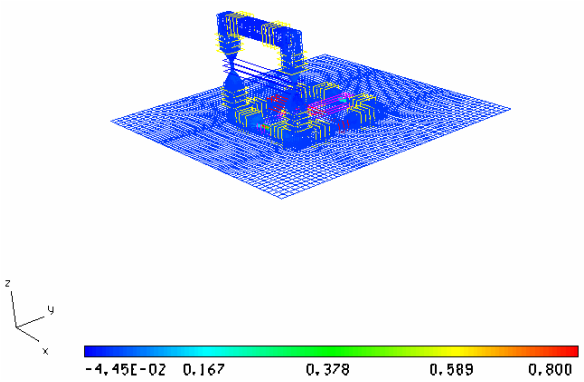
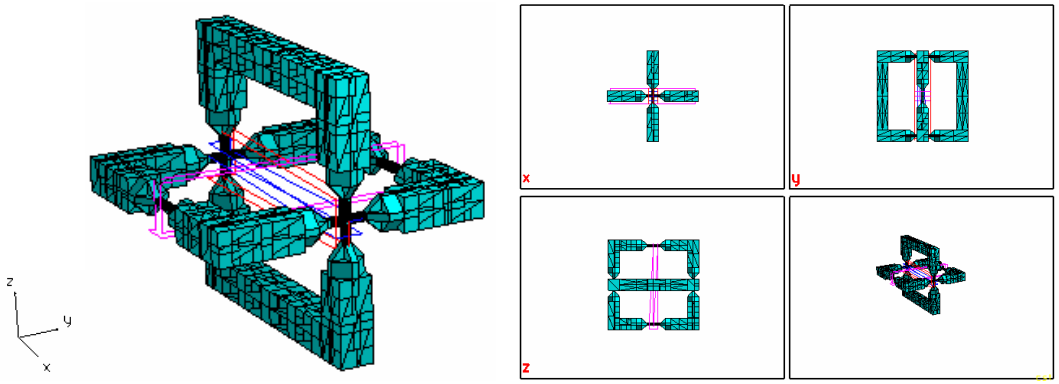


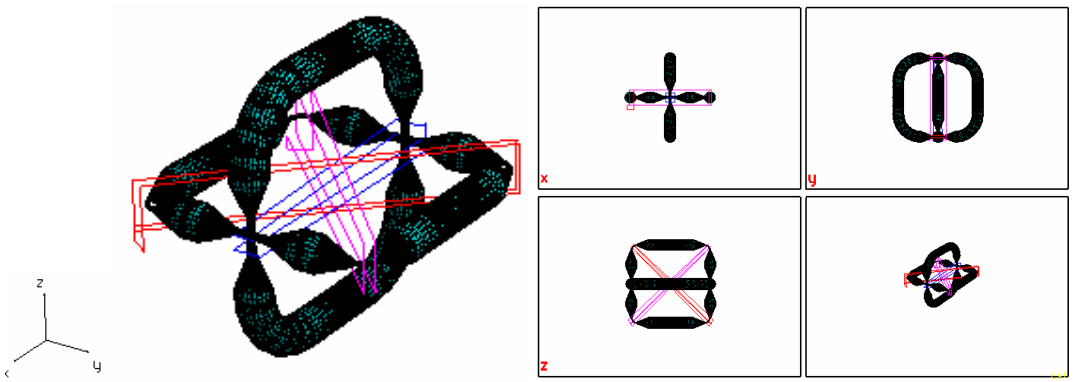
Figure 6.30 Magnetic Flux Density Distribution (Bsat = 0.8 T, Iexc = 35 uA).



(a) (b)

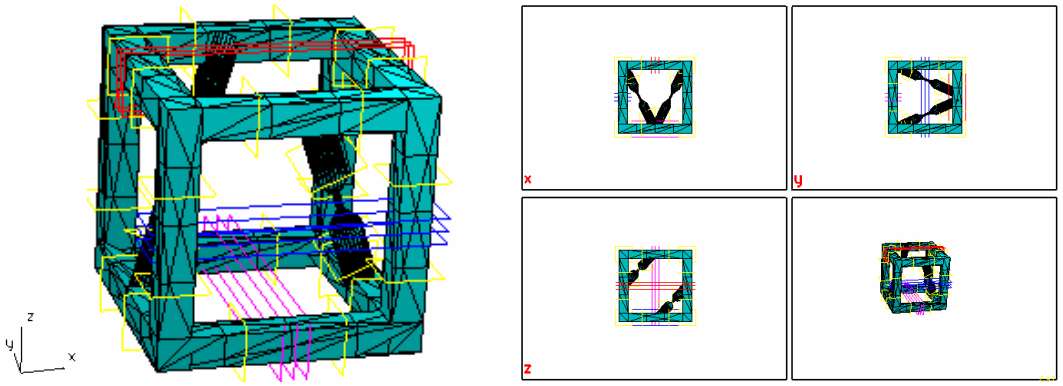
Figure 6.31 3-Dimensional Sensor No. 2 (a) 3-D Model (b) XYZ Projections.

The sensor in Fig. 6.31 saturates at 0.8 T for Iexc = 19 uA, due to the intercepting xy and xz planes cross. The sensitivity is 59 uV/nT. Winding the y- and z-axis sensor coils on top of each other decreases immunity to interference. The y- and z-axis directivity is reduced, due to the slot in the middle of the coils. Proper winding yields to adequate z-axis results for the model in Fig. 6.32. Angled fields could affect z-axis measurements. For 6 and 2 cone-link arrangements in the xy and xz planes, respectively, Iexc = 7.8 uA. The design exhibits non-linearities and strong demagnetisation effects at its quarter-circular edges.



(a) (b)

Figure 6.32 3-Dimensional Sensor No. 3 (a) 3-D Model (b) XYZ Projections.



(a) (b)

Figure 6.33 3-Dimensional Sensor Final Design (a) 3-D Model (b) XYZ Projections.

The sensors are coiled around two unused sides, in Fig. 6.33. Optimisation is applied by joining the bottom right-side with the front topside, and the bottom left-side with the back topside middle sections, using a cone-link section. An excitation coil of 28 turns saturates the core at 0.8 T for Iexc = +/- 60 mA, in Fig. 6.34. The balanced distribution of the field strength's phase distribution throughout the core is in Fig. 6.35.

The x-axis B distribution for an external field of 100 uT, 60 us after the commencement of the transient response analysis, is in the z-axis diagram of Fig. 6.36 (Bsat = 0.68 T).

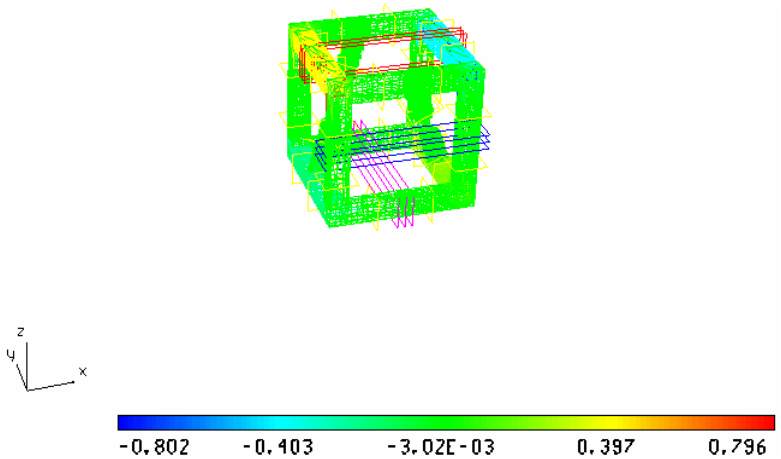


Figure 6.34 3-D Sensor B Distribution (Bsat = 0.8 T, Iexc = 60 mA).

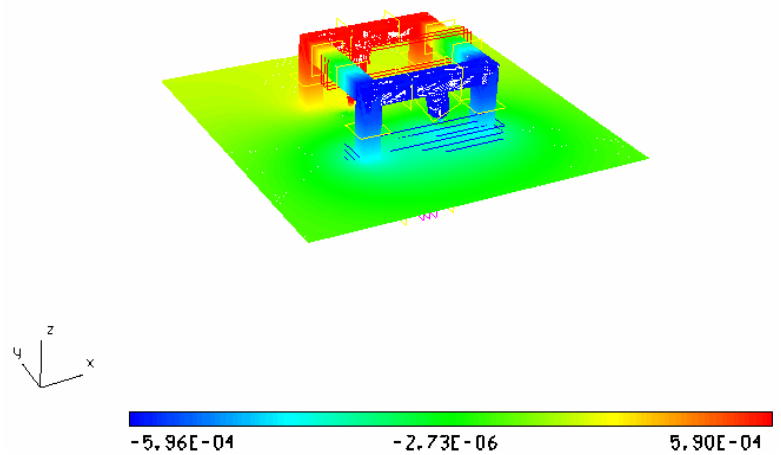


Figure 6.35 3-D Him Phase Distribution.

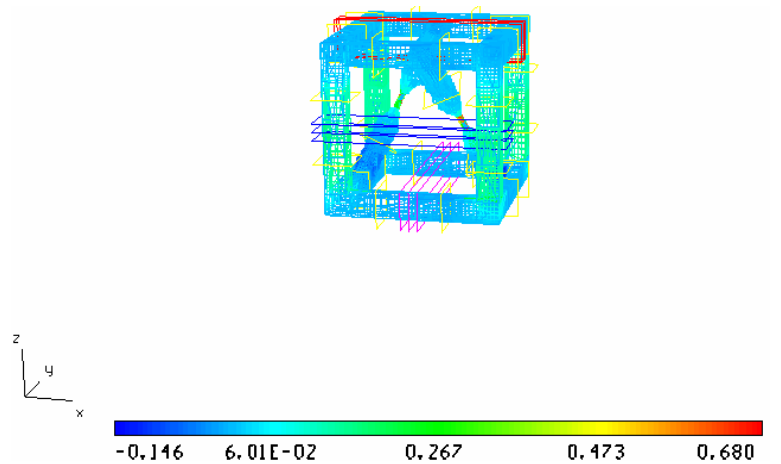


Figure 6.36 Magnetic Flux Density Distribution (Bsat = 0.68 T).

The sensitivity is 163 uV/nT, in Fig. 6.37. The y-axis output for Bext = 50, 100 and 150 uT is in Fig. 6.38. Vpp = 25.2 mV for B = 150 uT. The z-axis response for Bext = 250 and 300 uT is in Fig. 6.39. The x-axis directivity plot is in Fig. 6.40 for N = 1, 5, 10, 15, 20 and 24.

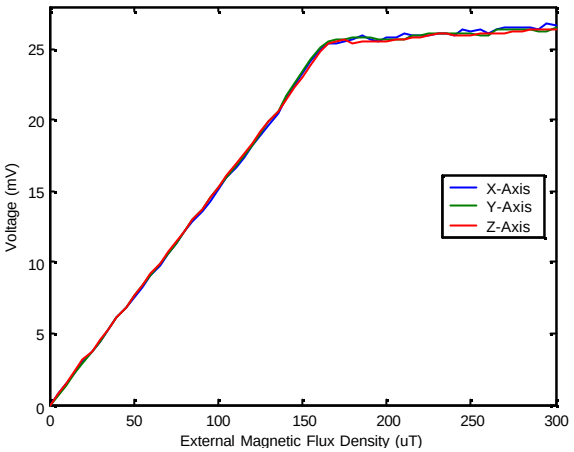


Figure 6.37 3-D Sensor's Sensitivity Diagram.

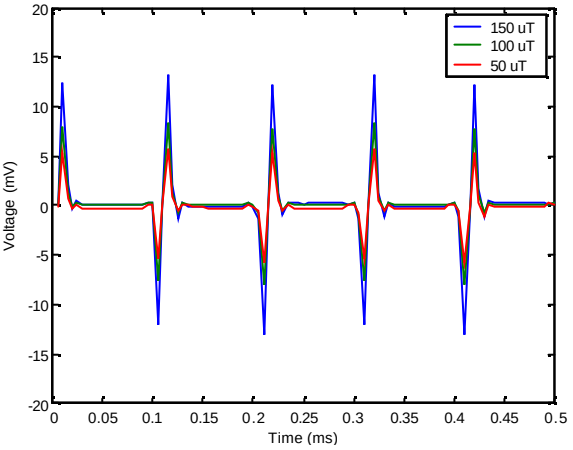


Figure 6.38 3-D Sensor's Output Response for B = 50, 100 and 150 uT.

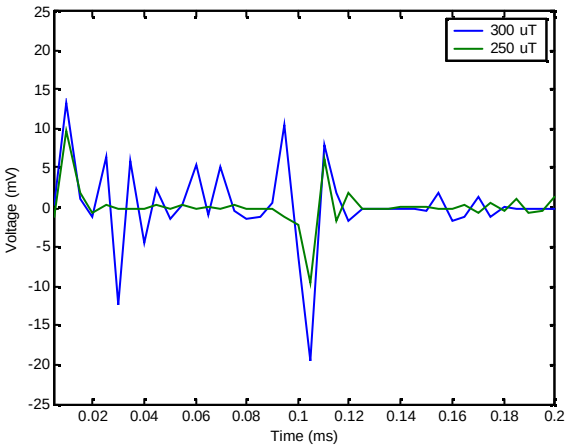


Figure 6.39 3-D Sensor's Output Response at Saturation for B = 250 and 300 uT.

The B (H) characteristic curve for the tri-axial sensor is in Fig. 6.41.

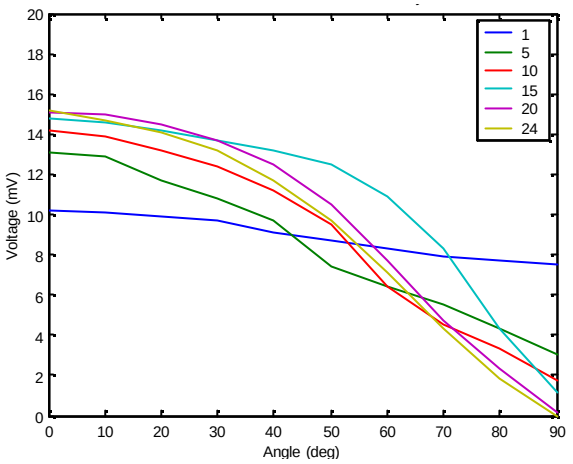


Figure 6.40 3-D Sensor's Directivity Diagram for B = 100 uT.

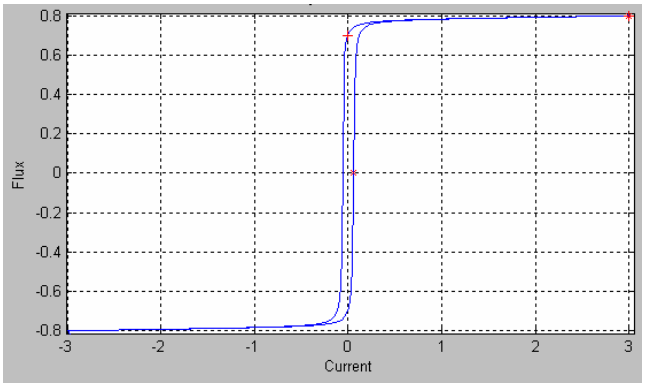


Figure 6.41 Tri-Axial Sensor's Magnetisation B(H) Curve (T(A/m)).

Magnetostatic simulations signified that under no influence of the external environment, the tri-axial sensor saturates for an excitation current of 60 mA at 0.8 T. The transient analysis results indicated that for an external field of 150 uT, the sensor has Vpp of 25.2 mV. The sensor's sensitivity is 163 uV/nT. The sensor has optimum directivity results in all directions for N equal to 24.

6.9 Sensor Design Experimental Results

The prototype core on the left of Fig. 6.42 is assembled and packaged using an excitation coil of 240 turns arranged into 8 coils in series each of 30 turns. The sensor coil has 50 turns of 0.1 mm Cu. The prototype is a combination of a race track of eight layers of 250 um. The two sensors on the right have an aspect ratio of three, suitable for single-axis measurements. The y-axis of the first core on the left could accommodate a second sensor coil for the y-dimension.

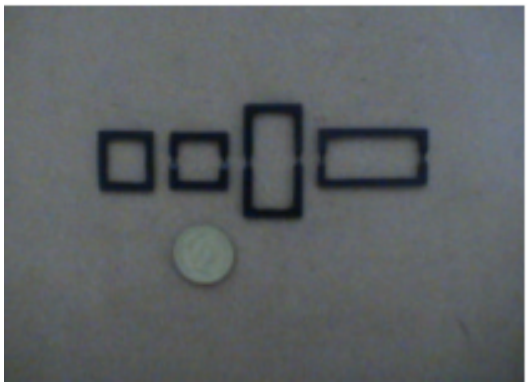
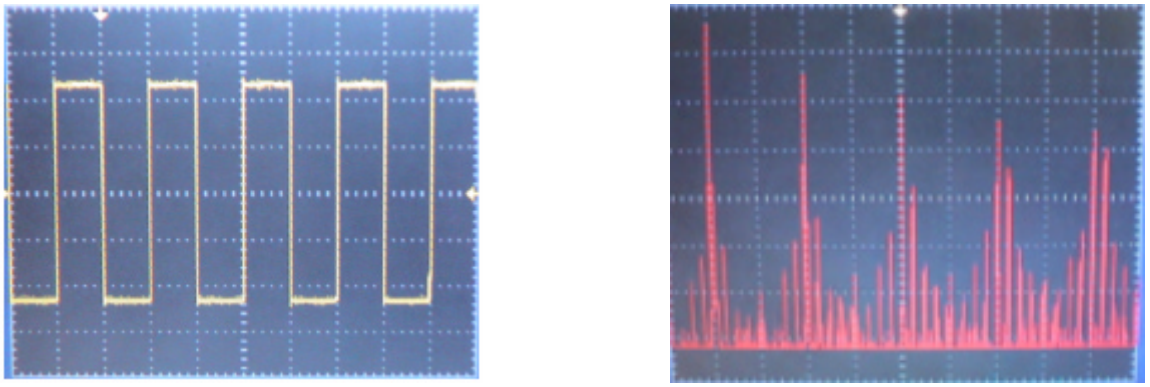


Figure 6.42 Prototype Fluxgate Sensor Cores.



(a) (b)

Figure 6.43 Excitation Waveform in (a) Time (b) Frequency Domain.

A 5 V, 5 KHz squarewave of +/- 250 mA is driving the excitation coil, as in Fig. 6.43 (a) (1 V/div, 100 us/div) and Fig. 6.43 (b) (10 dB/div, 5 KHz/div). When no current is applied the core absorbs the incoming wave. The induced magnetic flux density is in the range of -1.55 uT to 0.246 uT. At saturation the core resumes the Bsat value of 0.8 T.

An example snapshot is in Fig. 6.44, while the sensor is operated within the linear magnetisation region towards saturation with a peak-to-peak voltage of 4.4 mV. In parallel type sensors a BPF distinguishes the 2nd harmonic from the 1st and 3rd harmonics. Using a core such as in Fig. 6.42, all odd harmonics are nullified without magnetic filtering and a LPF at the 3rd harmonic extracts the 2nd harmonic, as in Fig. 6.45.

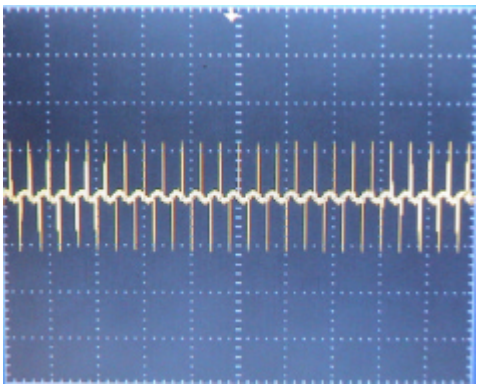


Figure 6.44 Driving the Sensor within the Linear Magnetisation Region.

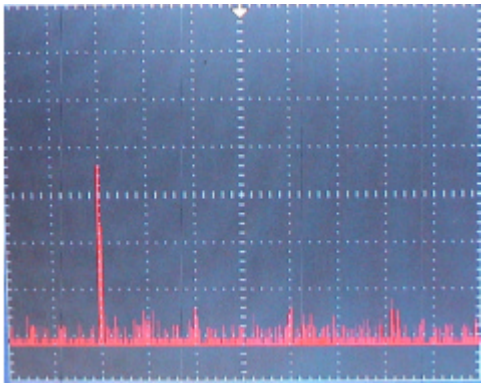


Figure 6.45 LPF Frequency Response.

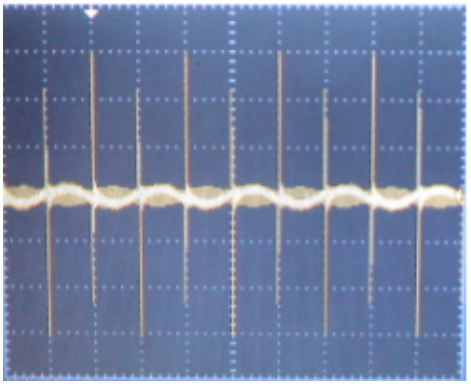


Figure 6.46 Sensor's Output Response for B = 60 uT.

The filtered output at saturation is in Fig. 6.46. A 12 mV output is obtained for a field in the range of 60 uT. The output for a 100 uT external field is 15 mV. The sensitivity of the sensor is 189 uV/nT, as in Fig. 6.47. The core consumes 258 mA in the premagnetisation stage.

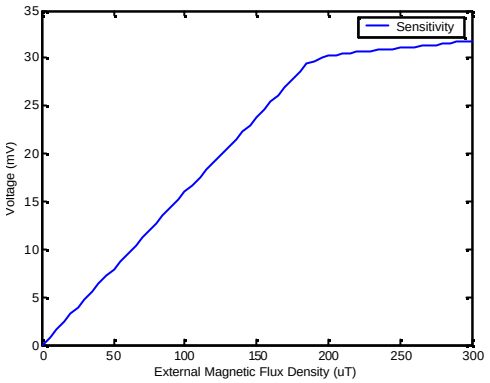


Figure 6.47 Sensor's Sensitivity Diagram.

6.10 Experimental Results for the Optimised Sensor

The second core on the left in Fig. 6.42 saturates at 0.8 T for an excitation current of 60 mA. A multi-meter is serially connected between the inverter and excitation coil. At premagnetisation the core draws 60 mA, being reduced to 0 mA at saturation, than to -60 mA, back to zero and to 60 mA to complete the path, as explicitly shown in Fig. 6.48. Vpp is 9.65 mV for an external field of 60 uT, in Fig. 6.49.

Figure 6.48 Core Excitation from Premagnetisation to +/- Magnetic Saturation.

The sensor is tested for a varying external field and the link's sensitivity for the bottom x-branch is 197 uV/nT. Overall, the sensor has sensitivity of 151 uV/nT. The noise spectrum for the optimised sensor is in Fig. 6.50 for the range 0 - 25 Hz (2.5 Hz step) and 5 dB/div.

The spectrum is produced by averaging 128 overlapped samples. The noise spectral density is $4.7\,\mathrm{pT}/\sqrt{\mathrm{Hz}}$ at 1 Hz. The rms noise level is 9.76 pT for the frequency range of 100 mHz - 16 Hz or 10.8 pT up to 50 Hz. The time domain noise spectrum of the optimised sensor is in Fig. 6.51. The scale is 50 s/div and 20 pT/div. The plot is averaging 128 overlapped samples. The peak-to-peak value is approximately 10 pT. The 50 s gap in the overlapping results is because the snapshot was in real-time.

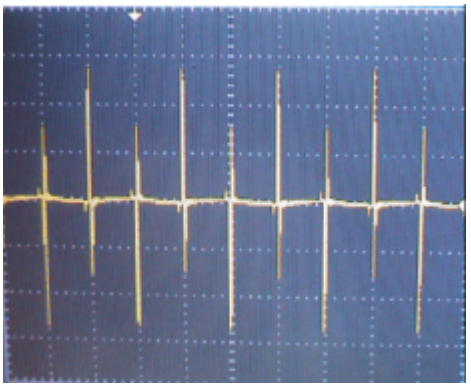


Figure 6.49 Sensor's Output Response for B = 60 uT.

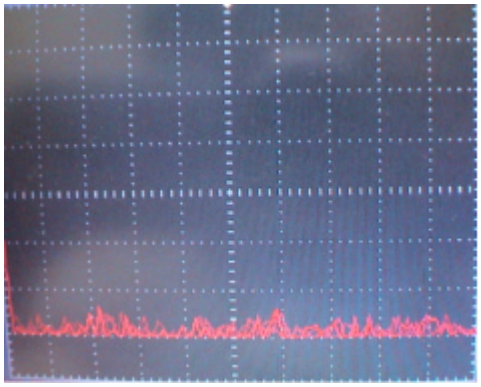


Figure 6.50 Frequency Domain Noise Spectrum for the Optimised Sensor.

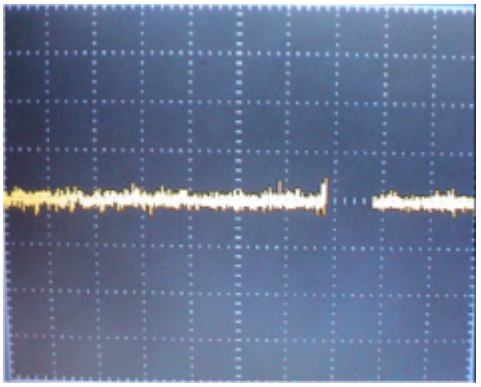


Figure 6.51 Time Domain Noise Spectrum for the Optimised Sensor.

6.11 Conclusion

The chapter described the specifications, system analysis and design methodology for engineering a basic fluxgate sensor and its optimised version.

The macroscale optimised sensor saturates for an excitation current of only +/- 60 mA, which is 4 times less the initial specifications of 250 mA. This leads to a reduction in power consumption by a factor of 16. The air gap fringing flux in the optimised region is 10^{-6}. The sensor has a guaranteed sensitivity of 100 uV/nT and an output Vpp of 19.45 mV to amply cover the Earth's magnetic field variation. The sensor has a maximum sensitivity of 151 uV/nT.

The tri-axial fluxgate sensor is built by an assembly of three single-axis sensors [212] or by manufacturing the tri-axial compact core accommodating all three sensing dimensions. In this way, the Dimagoras specifications and datapath processing requirements are determined.

Chapter 7 proceeds to the magnetometer's remaining hardware design.

Chapter 7.

The Novel Digital Magnetometer for Oracular upper-Atmospheric Studies (DIMAGORAS): Hardware Design

7.1 Introduction

The chapter describes the hardware design of the remaining Dimagoras system. The sensor determines the system's datapath requirements. Each sensor's output is amplified by 20 dB. A BPF tuned to 10 KHz reduces the BW to 4 KHz. The AGC functionality is by default hardware controlled and overridden by SDR commands. Three digital amplifier circuits provide gain control in the range of -20 - 70 dB. The differential outputs connect to three 3 MSPS ADCs. The ADCs are programmed in parallel. The 16-bits outputs are temporarily stored to a 512 x 32 FPGA FIFO.

An anti-aliasing FIR LPF, filters the FIFO contents to a matching 4 KHz BW, eliminating any higher frequency images of the sampled data. The filtered outputs are cross-correlated with the reference waveform, extracting the external magnetic field density of each channel. The results are UTC timestamped. An interpolation algorithm drives the programmable DAC with the cross-correlated data. The compensation coil is driven by the DAC LPF stage. A current of 1.02 mA, generates the 151 uT nullifying field. A programmable inverter provides the saturation current of +/- 60 mA.

The cross-correlated data are decimated to 10 Hz BW using a 3-stage decimator. The filtered results are converted to nT using a real-time numerical algorithm. The system's output is either the total field intensity or vector components. Data are temporarily stored into SRAM or real-time transferred via the UART, USB 2.0 or 10/100 Mbps Ethernet interface to host.

7.2 Pre-Amplifiers Design

The PA circuit for each channel is in Fig. 7.1 [213]. The closed loop frequency and phase response is in Fig. 7.2. The results for a +/- 30 mV (100 uT) squarewave and sinewave input are in Fig. 7.3. Each PA is tuned to 10 KHz. BW is 4 KHz. The voltage gain is 20 dB. The attenuation is 20 dB/decade. NF = 3.9 dB, IP3 = 31 dB and Zo = 50R.

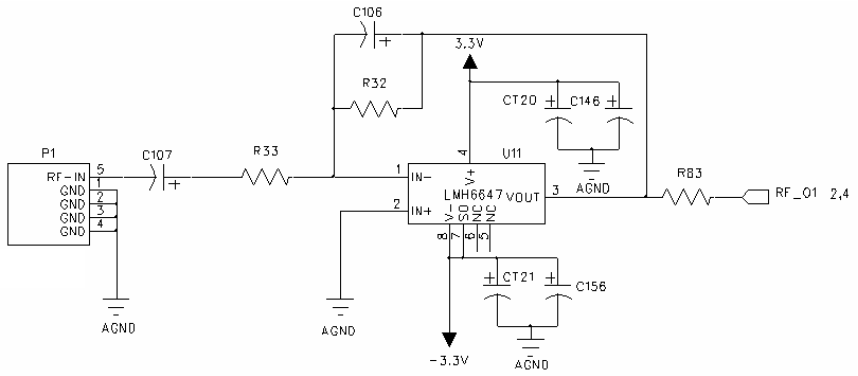


Figure 7.1 PA Schematic.

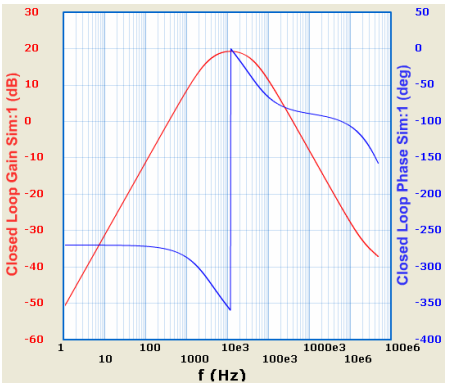
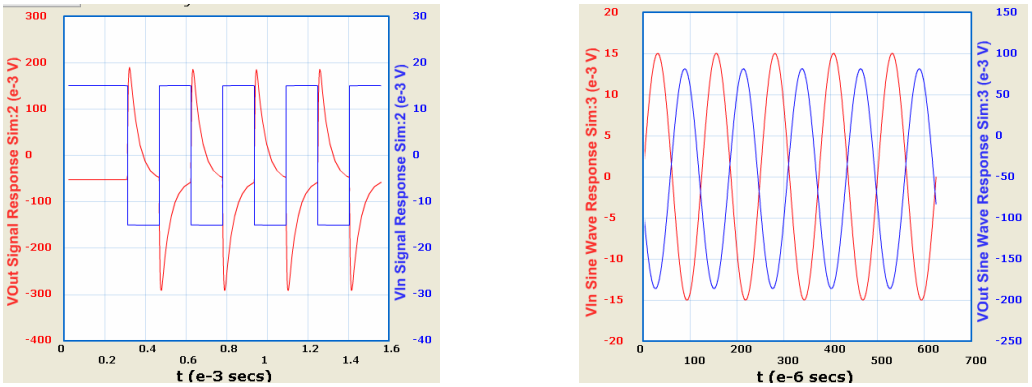


Figure 7.2 PA Frequency and Phase Response.



(a) (b)

Figure 7.3 PA Response for a (a) Squarewave or (b) Sinewave Input.

7.3 Digital Amplifier Design

The AGC circuit is in Fig. E.1. The PA's output 50R impedance is transformed to the AGC input impedance. An 1-4 RF transformer of 0.02 dB insertion loss is used. The AGC also high-pass filters the signal at 1 KHz. AGC ranges between -20 to +70 dB. Vmag and Vdbs pins are controlled by the 64-position AD5233 digital potentiometer in Fig. E.2 [214].

7.4 Analogue-to-Digital and Digital-to-Analogue Converter Design

The 3 MSPS AD7621 ADC circuit is in Fig. E.3 [215]. The ADC samples at 100 KHz. C12 LPFs the AGC output at 2.2 MHz. The output is in the 2's complements format. The FPGA programs the sampling frequency, /CNVST, /RD, /CS and reset inputs. The compensation coils are driven by the 16-bits DAC8534 DAC, in Fig. E.4 [216]. The compensation coils are winded next to the sensor coils and eliminate the sensors' fields. Feedback is controlled by R19. The LPF amplifier unloads the DAC, has a unity gain and 2 KHz cut-off frequency. Each compensation coil draws 1.02 mA, corresponding to 151 uT. The FPGA updates the DAC via the 25 MHz SPI interface, every 0.2 ms. At 10 Hz BW, oversampling increases resolution to more than 16-bits. Default resolution is 2.33 nT/bit.

7.5 Excitation Driver Power Electronics Design

The excitation coils are driven to saturation by the power stage of Fig. E.5, [108] and [67]. The FPGA output /INV1 transmits the 5 KHz squarewave to the single-stage inverter.

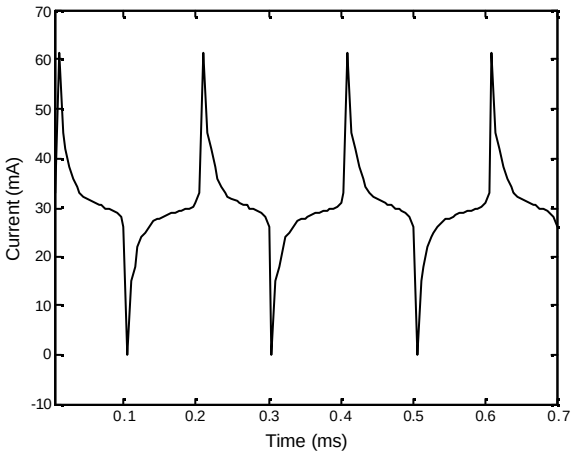


Figure 7.4 Excitation Coil Saturation Current.

The NMOS and PMOS transistors have matched switch-level RC delay and path effort. The diodes across the transistors, discharge static charge accumulation. The 1 mH ferrite bead, converts voltage into current for the LC-tuned circuit formed by CT38 and excitation coils. The single-stage inverter current output is in Fig. 7.4.

7.6 UART Interfaces Design

The SN75LV4737A UART interfaces allow bi-directional communication between the GPS receiver and FPGA in Fig. E.6 and between the FPGA and host in Fig. E.7 [188]. The GPS and FPGA interfaces are configured as DCE and DTE, respectively.

7.7 10/100 Mbps Fast Ethernet Interface Design

The Ethernet interface, based on the Intel LXT970 transceiver is in Fig. E.8 [217]. Ethernet MAC controls reception and transmission of CSMA/CD data packets [218]. Within the 7-layer OSI model, Ethernet MAC is the data link layer, connecting the network to physical layer. 802.3 data format is used.

The Ethernet interface is in Fig. 7.5. The receiver and transmitter functions are in Fig. 7.6 and Fig. 7.7, respectively. The receiver decodes the received CSMA/CD data. Reception is aborted if the frame length is exceeded, an error has occurred or during reset. Rx_clk is 25 MHz for 100 Mbps operation. The Receiver includes the receiver buffer, address verification and matching circuit, FCS checker and SFD checker.

The transmitter transmits CSMA/CD data into an idle medium to avoid collisions. During a collision, data is retransmitted after a period proportional to the number of collisions. Transmission fails during excess deferral, frame length >1518 B, late collision or underrun. Excess deferral occurs during a less than 3036 B transmission period. Late collision occurs for a collision, soon after the first 512 bits are transmitted. Excessive collision occurs, for an over 15 times repeated collision. Underrun occurs when data are not available for transmission. Tx_clk is 25 MHz for 100 Mbps operation. The transmitter performs DMA accesses and consists of the transmission controller, FIFO, defer counter, frame length counter, collision counter, jam timer, random number generator, inter frame gap (IFG) counter, back off counter, CRC generator and data multiplexer.

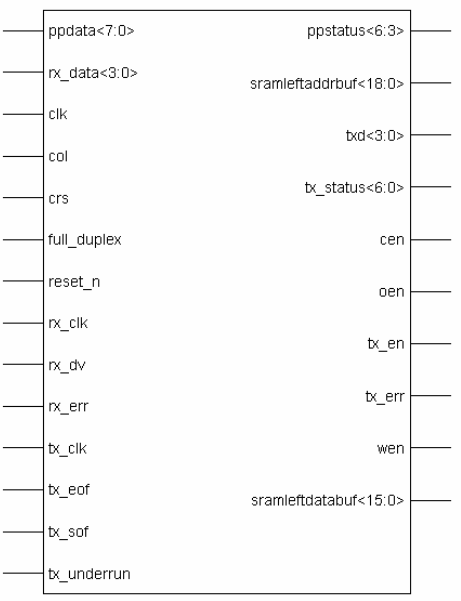


Figure 7.5 Block Diagram for the 10/100 Mbps Fast Ethernet Interface.

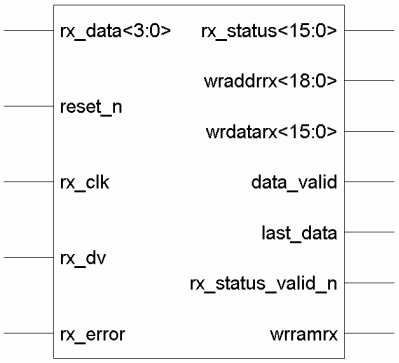


Figure 7.6 Block Diagram for the Ethernet Receiver.

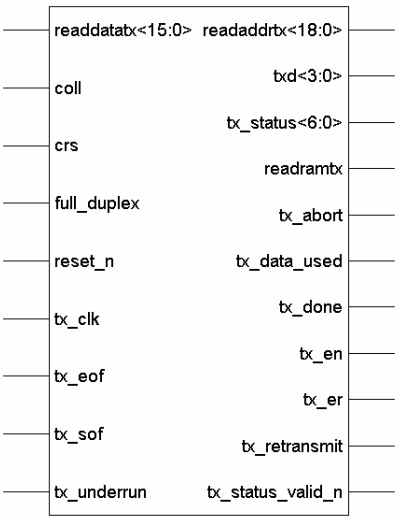


Figure 7.7 Block Diagram for the Ethernet Transmitter.

7.8 16 Mbits SRAM Memory Interface Design

The 16 Mbits SRAM, based on the Samsung K6R4008C1C-J-C15 module is in Fig. E.9 [219]. SRAM is configured into two sets of 512 K x 16 bits. The access time of 15 ns is low, compared for instance to the 70 ns access time of the 512 K x 8 bits Samsung K6T4008C1B-VB70 [220]. The memory is accessed in many ways [221]. For the default integration time of 1 s, the UTC timestamped data are stored for up to 144 hours. Depending on the ISA commands initially issued, if the zero times overlapping data are not acquired, the values are overwritten at 1 Hz rate or the routine halts.

7.9 FPGA Hardware Design and Analysis

Dimagoras is based on the XC3S1500-4FG456 FPGA [222]. Three FPGA schematic pages are in Fig. E.10 – E.12. Data are stored into a 512 x 32 dual-port FIFO [145]. The FIFO data are multiplexed through the matching FIR filter. The anti-aliasing filter matches the PA's 4 KHz BW and any higher frequency images of the sampled signal are removed. The filter has 16 coefficients. The maximum group delay at resonance is 1.6 ms. For a stable filter, the minimum stopband frequency is 18 KHz for a passband frequency of 15 KHz. The order is increased to 46 for a Direct Form II Transposed architecture. The maximum group delay at resonance is 6.6 ms. The DC gain is 1. The filter's outputs are de-multiplexed to three cross-correlators. The cross-correlator performs a peak-power detection algorithm. 100,000 cross-correlated values are integrated for a default period of 1 s. Only 10,000 results have a value other than zero.

The cross-correlated values are fed to the interpolator, which generates the appropriate DAC values. The interpolator matches the DAC's rate using a sample rate expander. The output of the up-sampled waveform is LPF filtered to reject any image frequencies created by the up-sampling process. The process is given by eq. (7-1) [223]:

$$c(r) = \sum_{N=0}^{N-1} f(N)g(r-N) \qquad (7\text{-}1)$$

where, c (r) is the LPF output function, f (N) the LPF transfer function and g (r – N) the up-sampled function. The up-sampled function equals:

$$g(r) = \begin{cases} x(r / L), r = 0, \pm L, \pm 2L... \\ 0 \end{cases} \quad (7\text{-}2)$$

where, x (r) is the cross-correlated result and L the interpolation rate.

However, some concerns are raised regarding the interpolation and DAC processes. Firstly, the theory of interpolation applies directly to a DAC with no internal memory, updated every 10 us. If such a DAC device was used, the up-sample rate is 100,000 for 1 s integrated values. Therefore, reprogramming the UTC referenced integration time requires reconfiguration of the interpolator. This increases the effort in designing the interpolator. If the sum of the two instantaneous maximum cross-correlated values is transferred once per excitation cycle, the up-sampling rate reduces to 20, yielding to a reduction by a factor of 5000. The circuit requires less effort to design. Therefore, x (r) in eq. (7-2) is replaced by:

$$x(r) = \frac{1}{N} \sum_{n=0}^{N-1} y(n)w(n) = \sum_{n=0}^{1} y_{max}(n)w_{max}(n) = \sum_{n=0}^{19} y(n)w(n) \quad (7\text{-}3)$$

where, y (n) is the FIR output and w (n) the reference waveform. Secondly, since the sensor consists of three macroscale optimised axial sensors, three interpolators and three DACs are initially required. Each interpolator and DAC is run by a different cross-correlated value. Since the purpose of the circuit is to nullify each sensor's field, without inducing any electromagnetic imbalance, a single value is transmitted instead. The comparison between the cross-correlated results is expressed by eq. (7-4).

$$x(r) = \begin{cases} \sum_{n=0}^{19} y_{Bx}(n)w(n), & B_x > B_y \cup B_z \\ \sum_{n=0}^{19} y_{By}(n)w(n), & B_y > B_z \cup B_x \\ \sum_{n=0}^{19} y_{Bz}(n)w(n), & B_z > B_x \cup B_y \end{cases} \quad (7\text{-}4)$$

The DAC8534 is programmed with an initial set of 20 values and cycles through them. It is updated once per excitation cycle with the result of eq. (7-4).

7.9.1 CIC Decimator Design

Further bandwidth reduction can be achieved at the FIR filter's or cross-correlator's output. IIR and FIR simulation results for the former case are in Fig. 7.8. The required frequency response is not provided by an IIR filter. A 40,815 coefficients FIR filter implementing the Window Kaiser function is in Fig. 7.8 (d). The high sampling rate compared to bandwidth makes the realisation of such a filter impossible.

Decimation means disregarding data. Since losing data at the beginning of the digital domain is not desired, a similar approach is followed, as in Priamos. At the DDC re-sampler stage the data are up-sampled, FIR filtered and down-sampled to match the rate of a data communications protocol. Re-sampling is a mixture of interpolation and decimation.

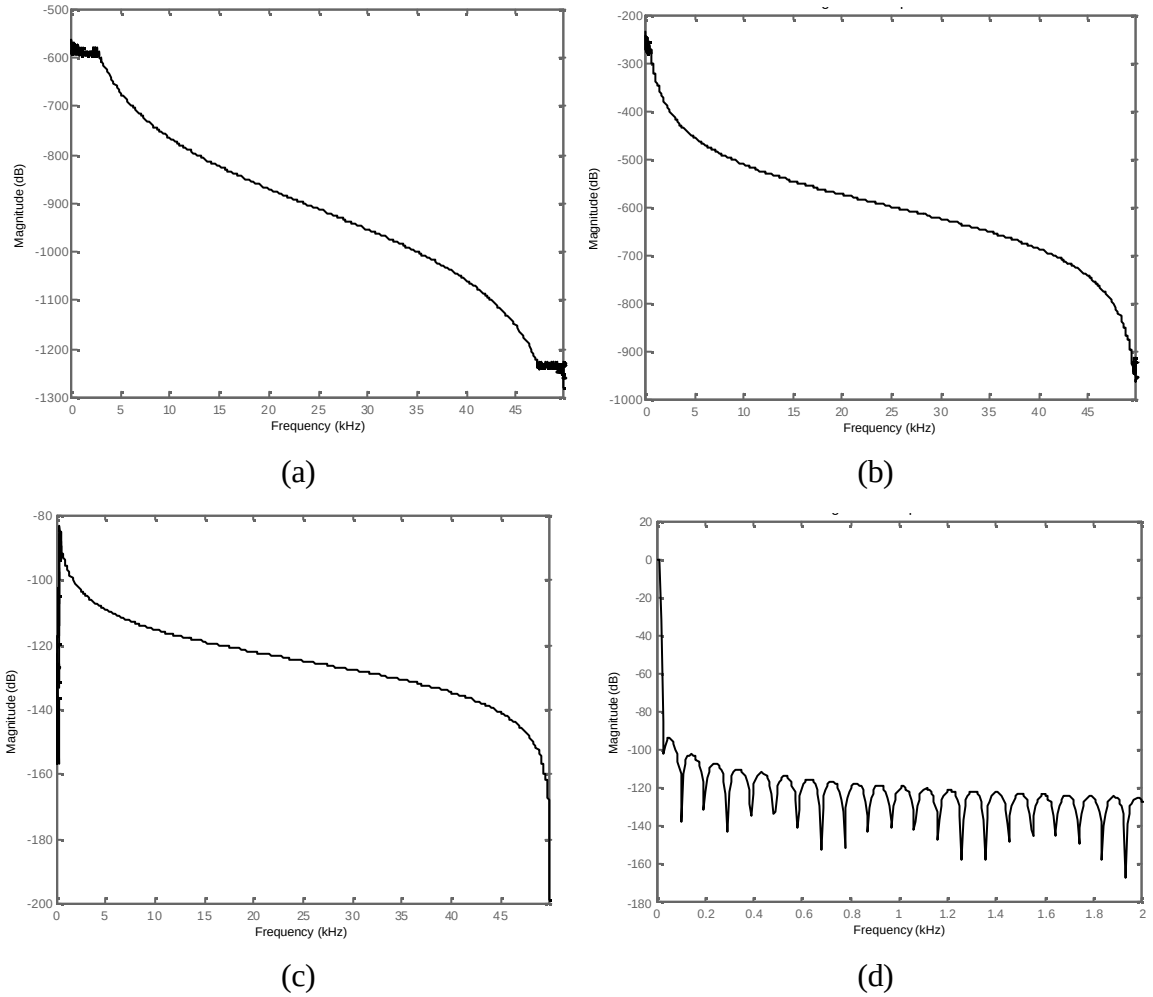


Figure 7.8 (a) IIR Butterworth (b) IIR Chebyshev I (c) IIR Chebyshev II (d) FIR Kaiser, LPF Frequency Response (BW = 10 Hz).

A single- or dual-stage decimator yields to high group delay. The solution is in the range of 3 to 4 stages. Adequate results were obtained for 3-stages, as in Fig. 7.9 and 7.10. The cut-off frequency for each stage is 1.2 KHz, 38 Hz and 10 Hz. The DC gain for each stage is 1. The group delay is 63 ms. Transition between sampling rates results in losing some data until filter recovery, since it corresponds to a transition in time.

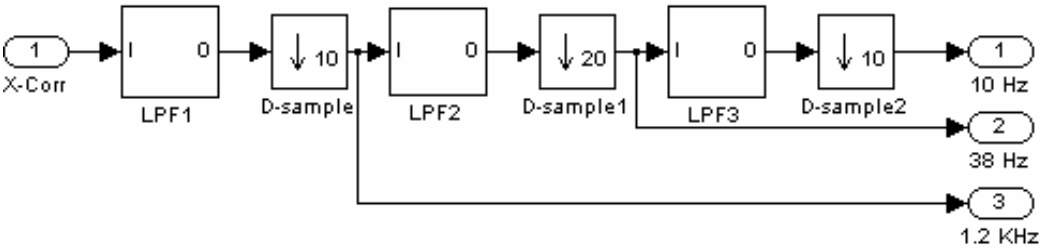
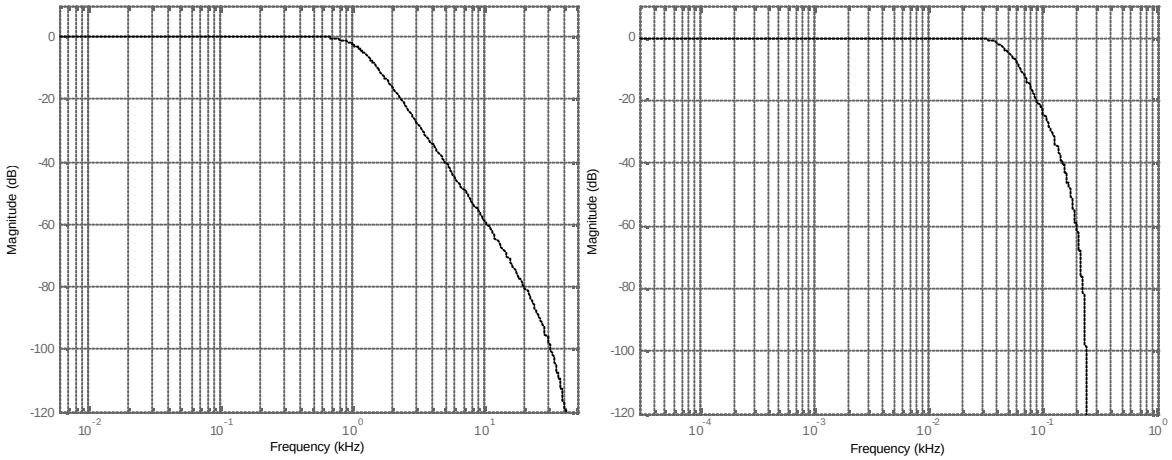
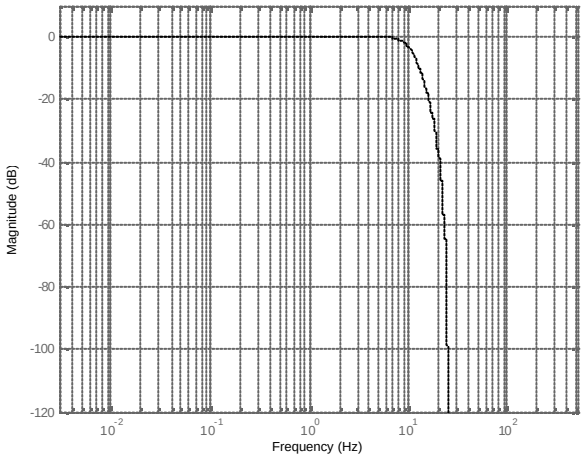


Figure 7.9 3-Stage Decimator Design.



(a) (b)



(c)

Figure 7.10 Decimator's Bode Plot for (a) 1.2 KHz (b) 38 Hz (c) 10 Hz BW O/Ps.

7.9.2 Power to nT Converter Design

The system outputs the UTC timestamped magnetic flux density values directly in nT. This constitutes a reduction in terms of software development time. Calibration and scale adjustment software routines seen in other systems are eliminated. The power to nT curve for each axis is in Fig. 7.11.

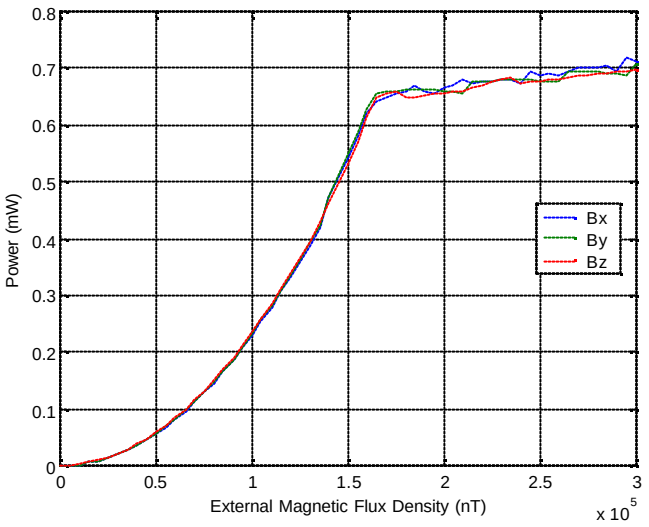


Figure 7.11 Power to nT Curves for the 3-D Sensor.

The circuit can be implemented digitally using a decoder or by storing the values directly into the embedded BRAM. Both solutions do not consider possible gain variations and adjustments are required before transmitting data to host.

A custom real-time numerical solution is proposed. A fundamental curve is produced by averaging the three curves. The error is less than 0.1 % and maximises in the saturation region. The derived curve is approximated by an x^2 function in the linear region and an error of 0 %. Magnetic saturation is approximated by a linear function. The adaptation of weights to known intermediate or maximum values relies on a look-up table (LUT) implementation.

7.9.3 Magnetic Field Total Intensity Calculator

The total intensity B_T of the magnetic field [222] is calculated by eq. (7-5):

$$B_T = \sqrt{B_x^2 + B_y^2 + B_z^2} \qquad (7\text{-}5)$$

where, B_x, B_y and B_z are the external magnetic field intensities towards the north, east and zenith directions.

The azimuth field intensity B_ϕ, included in eq. (7-5), is given by eq. (7-6):

$$B_\phi = \sqrt{B_x^2 + B_y^2} \qquad (7\text{-}6)$$

The inclination I and declination D are given by:

$$I = \arctan \frac{B_z}{B_\phi} \qquad (7\text{-}7)$$

$$D = \arctan \frac{B_y}{B_x} \qquad (7\text{-}8)$$

Dimagoras implements eq. (7-5).

7.10 Data Logging and Data Transfer

The system will join SAMNET after its completion. Data are recorded using one hour long ASCII files. A header is added to the data every minute. The filename format is ccDDMMYY.HH. The cc letters identify the system's name. YY, MM, DD and HH represent the year, month, day and UTC hour. No further processing is required, since the data are in nT. The host can remotely choose between the total intensity and the vector components, already expressed in magnetic coordinates.

7.11 Conclusion

The chapter described the hardware design of the remaining magnetometer system. Analysis is focused on the datapath processing requirements, to nullify the Earth's magnetic field and retain information regarding Space Physics events, based on the magnetic field variation captured by the macroscale optimised sensors.

In terms of hardware components, the programmable and reconfigurable Dimagoras system consists of: 3 PAs, 3 digital amplifiers, 3 ADCs, a DAC, a power stage, an external master oscillator, a GPS receiver, 16 Mbits SRAM, 2 UART ports, a USB 2.0 port, a 10/100 Mbps Fast Ethernet port, an FPGA and a power supply. Most of the components were developed for Priamos, restricting analysis to the new programmable interfaces.

The 3 PA circuits are tuned to 10 KHz, provide 4 KHz BW and a voltage gain of 20 dB. NF is 3.9 dB and the output impedance is 50R. The 1-4 RF transformer and a parallel resistor, convert the 50R impedance to the 1K2 input impedance of the digital amplifier. The amplifier has a programmable gain range of -20 dB to 70 dB and HPF the signal at 1 KHz. The 3 programmable AD7621 ADCs oversample at 100 KHz and LPF the signals at 2.2 MHz. The 2's complements outputs are multiplexed into a 512 x 32 dual-port FPGA FIFO.

An anti-aliasing FIR filter matches the 4 KHz BW and removes any higher frequency images of the ADC samples. The group delay is 6.6 ms. The filter's outputs are cross-correlated with the sensor's reference waveform, to detect each channel's peak-power. The cross-correlated products are interpolated and the DAC is updated once per excitation cycle. The DAC circuit nullifies the Earth's field, so that the field variation due to Space Physics events is measured. Each excitation coil draws +/- 60 mA from the programmable inverter stage to drive the optimised core to saturation.

The field variation is UTC timestamped and decimated to 10 Hz BW. 38 Hz, 1.2 KHz and 4 KHz BWs are laterally generated and available for data logging. A real-time numerical algorithm converts power measurements to nT. The scale is programmable and measures the interaction between the complex solar wind-magnetospheric-ionospheric system and ground-based magnetometer systems.

Chapter 8.
Conclusion and Future Work

8.1 Conclusion

The thesis work provides an insight to a variety of research topics, including Space Physics Instrumentation, hardware, electronics, sensor systems, DSP and Radio Astronomy. Research methodologies from these areas were applied to design the Priamos and Dimagoras systems.

Chapter 3 describes the hardware implementation a dual-channel cross-correlator, typically found in correlated Radio Astronomy systems. The hardware correlator is seriatim incorporated into Priamos and Dimagoras. The designs of an 8-phase auto-switching dual-channel correlator and a free-input dual-channel correlator are presented, based on the implementation of the cross-correlation function for non-identical incoming signals.

The dual-channel system requires 95,000 equivalent NAND2 gates and the frequency of operation is 81 MHz. The circuit is downloaded to the 6,000,000 gates XC2V6000-5-FF1152-based ADM XRC-II Alpha-Data board, equipped with the XRM-IO146 module. The bi-directional communication between the FPGA and host is via the 32-bits/33 MHz PCI interface. Data acquisition and visualisation is performed using C/C++ and Matlab software, respectively.

Chapter 4 describes the feasibility study, RF Receiver Unit and peripheral hardware design for Priamos. The RF Receiver Unit consists of five functional areas: RF input and calibration, PAs, filters, digital amplifier and ADC circuits. The peripheral hardware consists of the programmable master oscillator and GPS receiver. The bi-directional communication between the GPS receiver and host is achieved via the USB 2.0 and 10/100 Mbps Fast Ethernet FPGA interfaces.

Chapter 5 describes the hardware design of the Priamos DSP Engine Unit. The DSP Engine supports over 300 SDR commands in hardware. Eight mega-functions are implemented into the XC3S1500-4FG456 device to programme or reconfigure the FPGA, RF Receiver Unit, GPS receiver, master oscillator, 16 Mbps SRAM and glueless USB 2.0 and 10/100 Mbps Fast Ethernet Interfaces.

Programmable features include: dual-DDC processing, auto-correlation, sampling frequency up to 250 MHz, integration time, UTC RTC timekeeping, UTC data timestamping, long UTC timestamped data storage up to 144 h etc. The DSP Engine Unit is independent of the antenna type being used and provides a fast prototyping platform for other Space Physics Instrumentation projects.

Chapter 6 describes the feasibility study and system analysis for Dimagoras. A novel applied design methodology for engineering low-power macroscale optimised fluxgate sensors for measurements of the complex solar wind-magnetospheric-ionospheric system is presented. The optimised sensor saturates for an excitation current of +/- 60 mA, four times less the initial 250 mA specifications. Power consumption is reduced by a factor of 16. The sensor's sensitivity is 151 uV/nT to amply cover the Earth's magnetic field variation. The tri-axial sensor is built by assembling three single-axis sensors. The sensor determines the Dimagoras datapath processing specifications.

Chapter 7 describes the hardware design of the remaining Dimagoras system, consisting of the following programmable or reconfigurable interfaces: PAs, digital amplifiers, ADCs, DAC, power inverter stage, master oscillator, GPS receiver, 16 Mbps SRAM, FPGA, UART ports, USB 2.0 and 10/100 Mbps Fast Ethernet.

The system samples the sensors' outputs and cross-correlates them with the reference waveform to detect each channel's peak-power. The cross-correlated results are interpolated using a custom algorithm, updating the DAC once per excitation cycle. The Earth's field is nullified and the field variation data, due to Space Physics events, are captured and UTC timestamped. The bandwidth is reduced to 10 Hz. A real-time numerical algorithm transforms power measurements to nT.

8.2 Further Work

The Priamos system design is completed. The novel applied sensor design methodology for engineering low-power macroscale optimised fluxgate sensors is verified. The hardware design and simulation of the remaining Dimagoras system is completed. A few remarks regarding Dimagoras are in the following sections.

8.2.1 Remodelling the Sensors using Metglas 2714A

A new material was recently found, which could improve the magnetometer's specifications. The Metglas 2714A [224] magnetisation curve is in Fig. 8.1. The magnetic flux density saturation value is 0.57 T, compared to supermalloy's 0.8 T. The basic Metglas 2714A fluxgate sensor would saturate at 159 mA, compared to supermalloy's 250 mA.

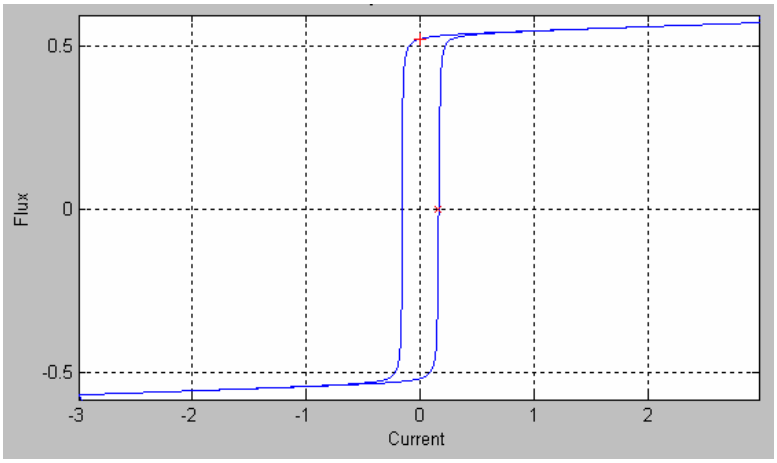


Figure 8.1 Metglas 2714A Magnetisation B (H) Curve (T(A/m)).

Applying the novel macroscale optimisation technique of Chapter 6, the excitation current can be reduced to an estimated value of 40 mA, compared to supermalloy's 60 mA. The core loss is 1 W/kg at 5 KHz. The power consumption is reduced by a factor of 39, compared to the basic supermalloy sensor.

8.2.2 Theoretical Calculation of the Earth's Magnetic Field

The system measures the aggregate disturbed magnetic flux density, due to the different ionospheric and magnetospheric events, plus any seriatim generated continental or sea fields, accounting for 2 - 3 % of the Earth's total magnetic field [222]. Another 2 – 3 % is due to the fields of the different materials at the Earth's crust. The remaining 90+ % is due to the Earth's core. The Earth's core field is included in the digital World Magnetic Model (WMM). The 2006 model and predictions until 2010 are published. WMM takes into account crustal magnetic fields, represented by a constant.

The contribution of magnetometers is not included in WMM. A new research study could use WMM and magnetometer data for short term predictions. The software development would couple the operation of Dimagoras. Since WMM takes into account the altitude variation, the predictive model would also apply to airborne magnetometers.

8.2.3 VLSI Considerations for Priamos and Dimagoras

The two projects could reach the VLSI stage within the next years. A mixed-signal approach is suited for the two projects [225]-[226]. The performance and frequency of operation are increased, while the power consumption and size are reduced. These factors are related to the slow speed of the FPGA's multiplexed switching matrices. The critical path of an implementation is longer than expected, due to the datapath routing through the different FPGA's embedded units.

Due to the low-levels of the received power an external antenna is still required for Priamos. Digital magnetometers have been implemented into ASICs for spaceborn applications [106]-[110]. Single- or dual-axis MEMS sensors can be embedded into ASICs. Tri-axial magnetometers utilise an external macroscale sensor. Due to the rapid development of the different processing technologies, it is worthwhile investigating the possibility of incorporating a tri-axial sensor into an ASIC. Investigation is required to determine the lowest limit of miniaturisation that the optimised sensor can be imposed to.

Appendices A-E

Appendix A Dual-Channel Cross-Correlator System

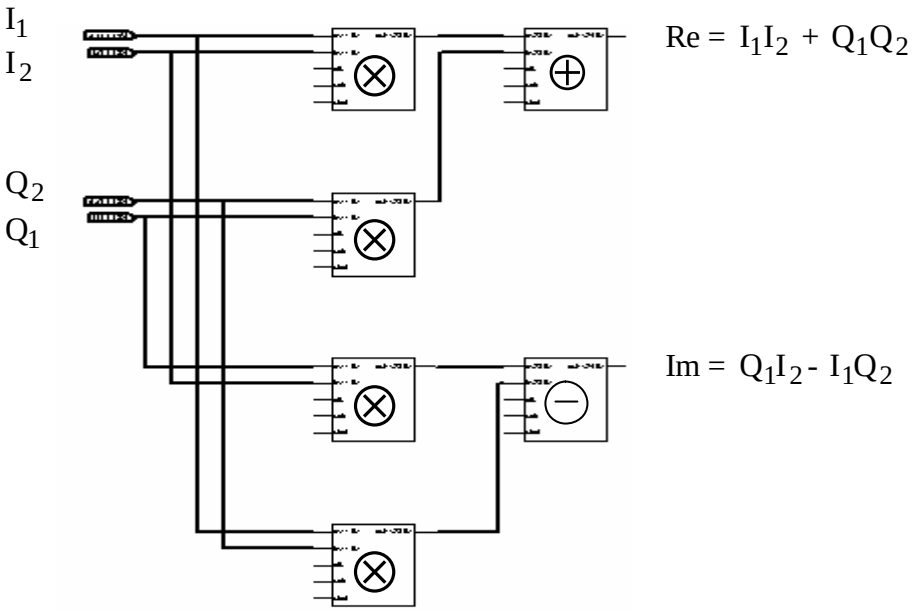


Figure A.1 Complex Multiplier's Block Diagram.

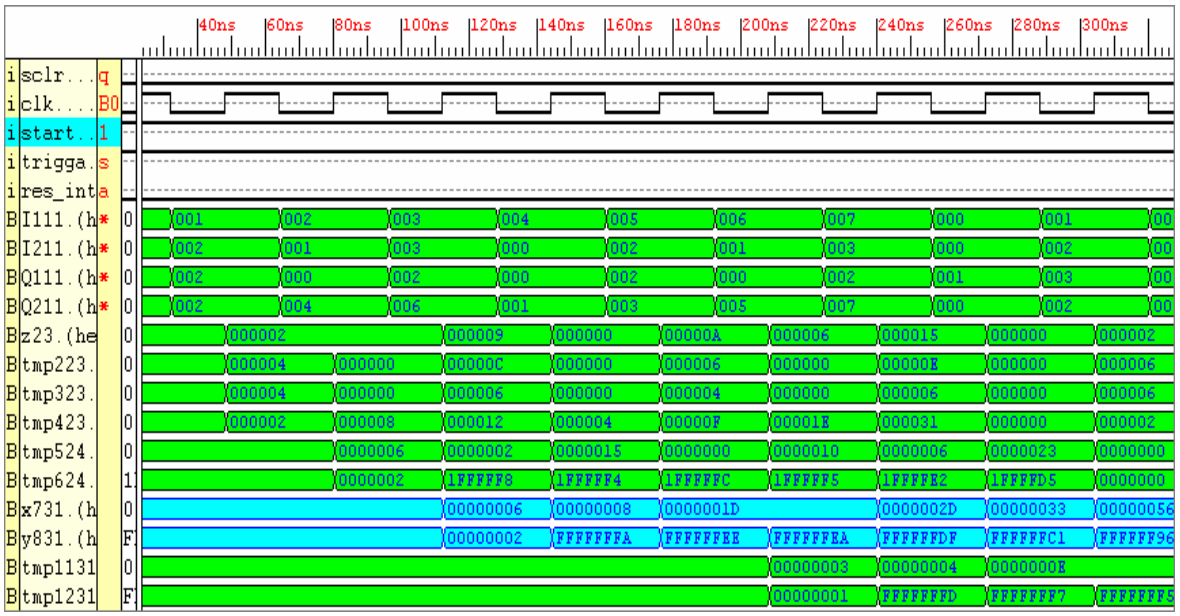


Figure A.2 Functional Simulation Results for the Cross-Correlator.

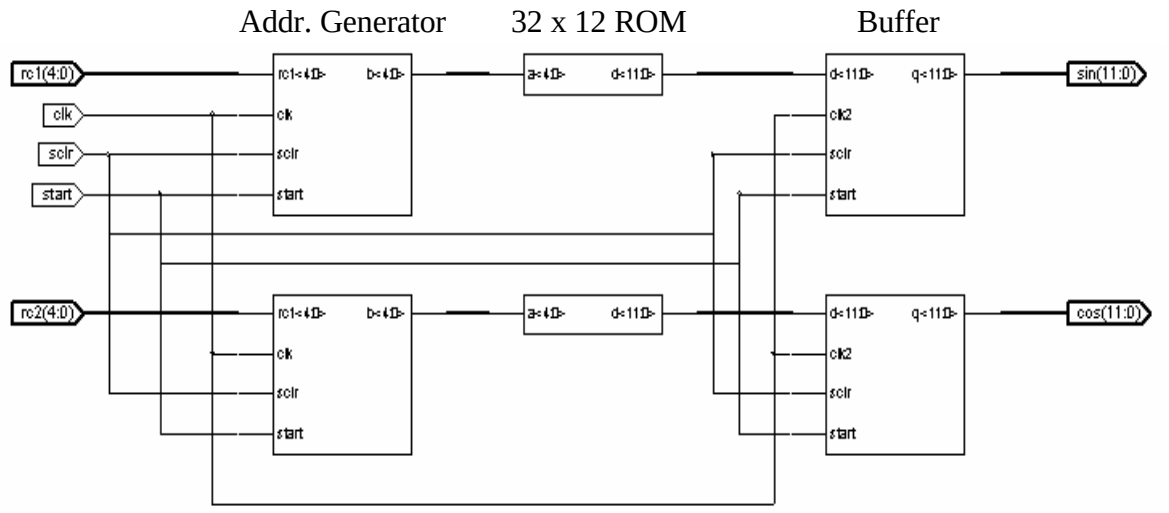


Figure A.3 Block Diagram of the Complex-Waveform Generator.

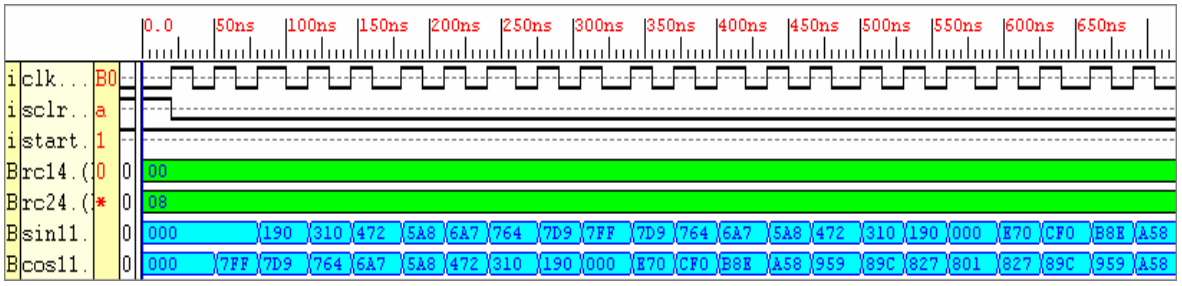


Figure A.4 Functional Simulation Results for the Complex-Waveform Generator.

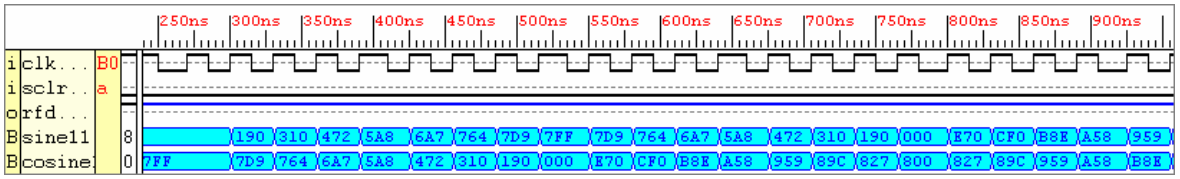


Figure A.5 Results for the 1st Channel DDS and Controller.

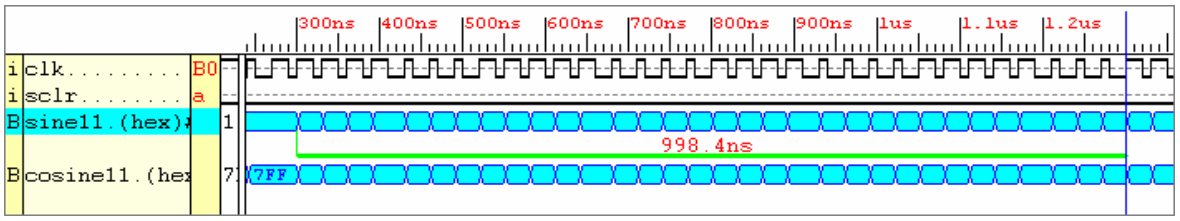


Figure A.6 Results for the 2nd Channel DDS and Controller.

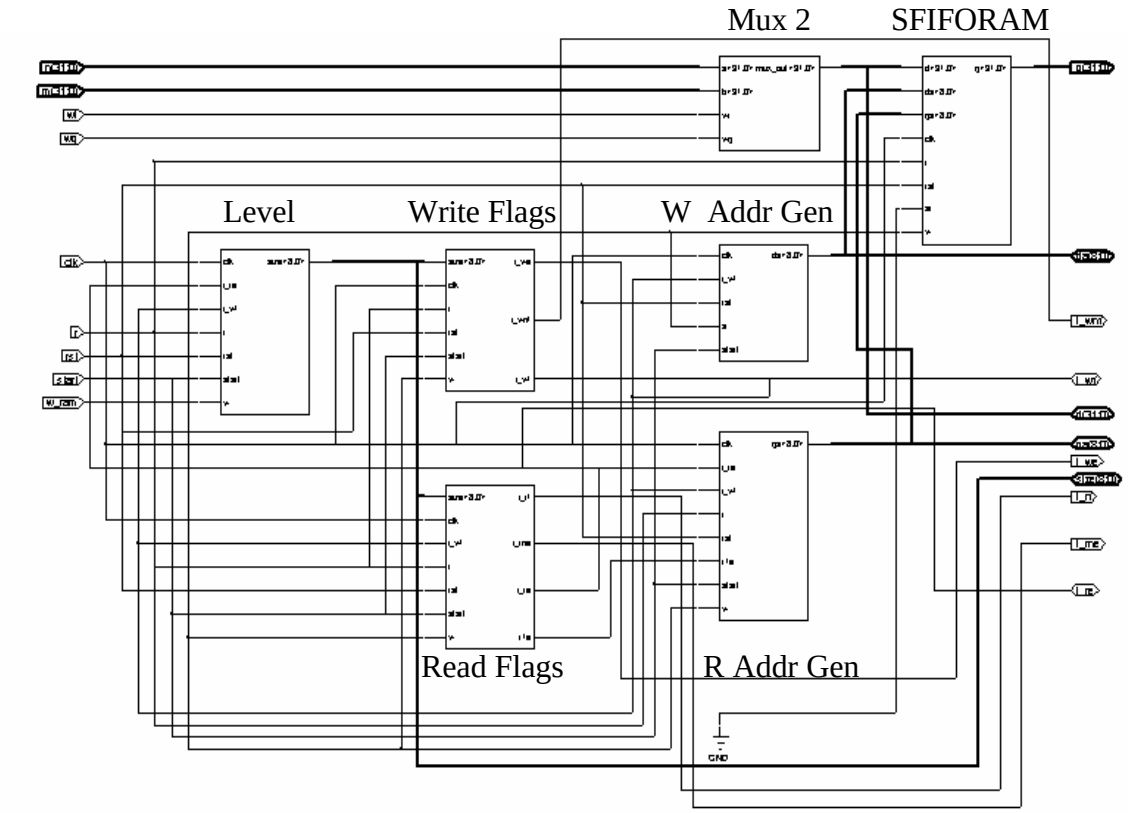


Figure A.7 Block Diagram of the FIFO Module and Controller.

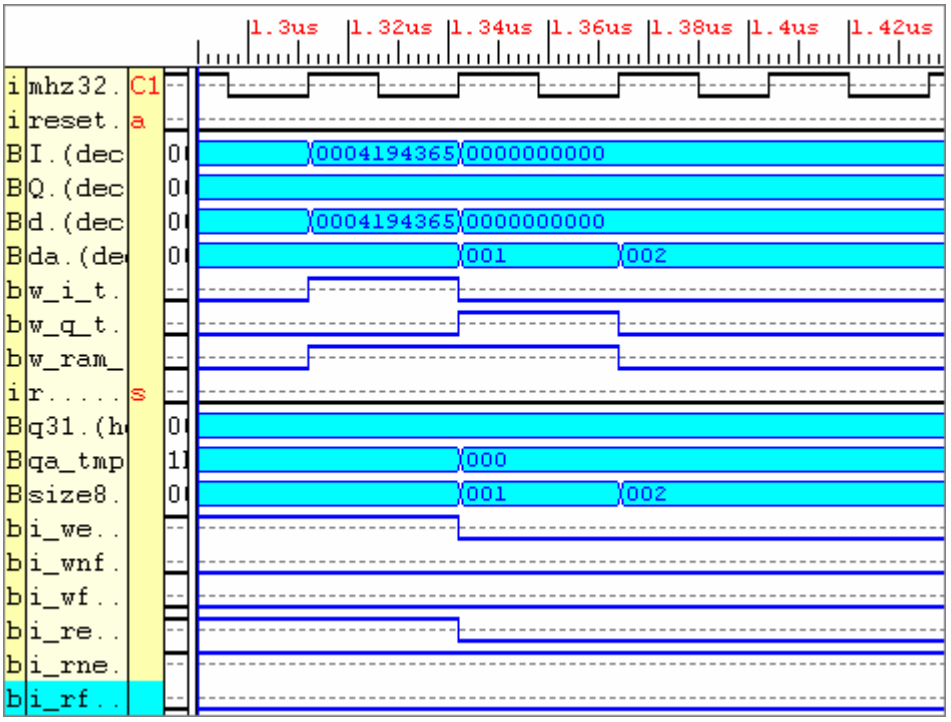


Figure A.8 Beginning of Write Cycle Results for the Cross-Correlator, FIFO and FIFO Controller.

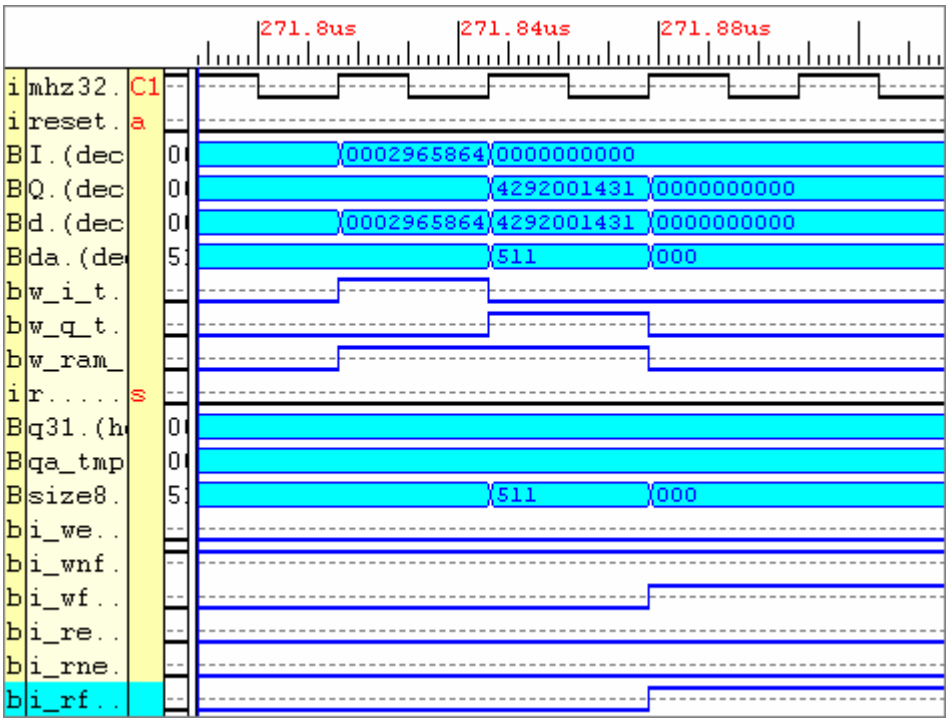


Figure A.9 End of Write Cycle Results for the Cross-Correlator, FIFO and FIFO Controller.

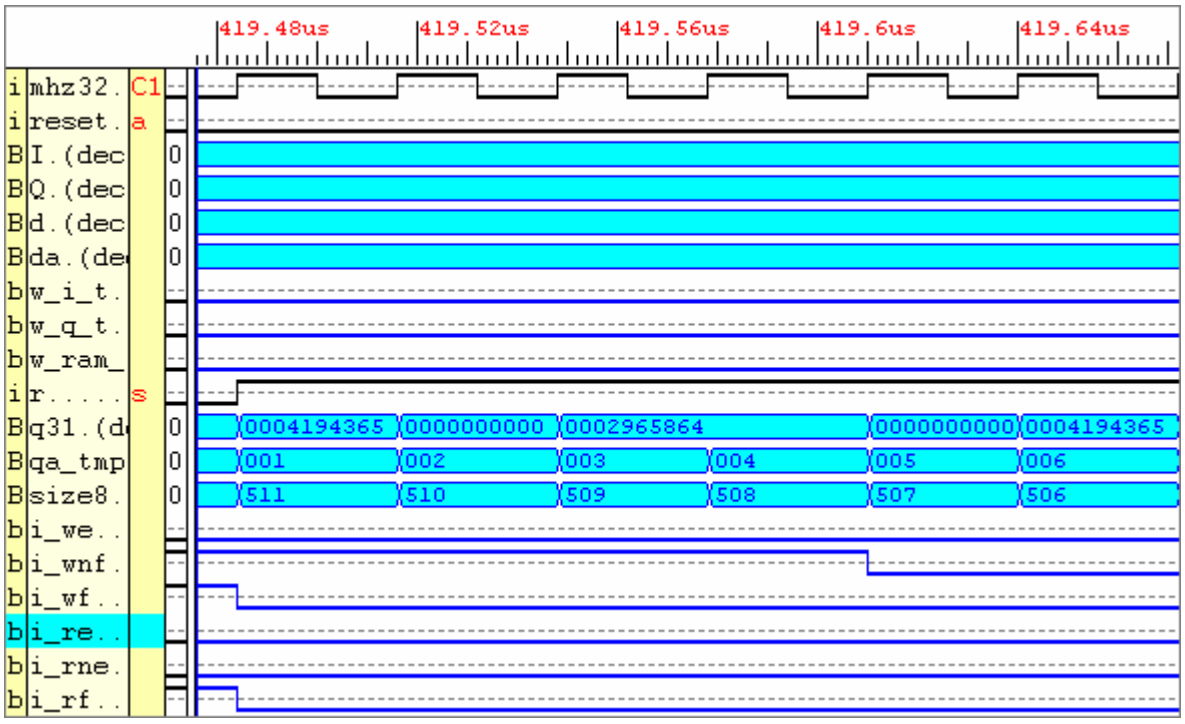


Figure A.10 Beginning of Read Cycle Results for the Cross-Correlator, FIFO and FIFO Controller.

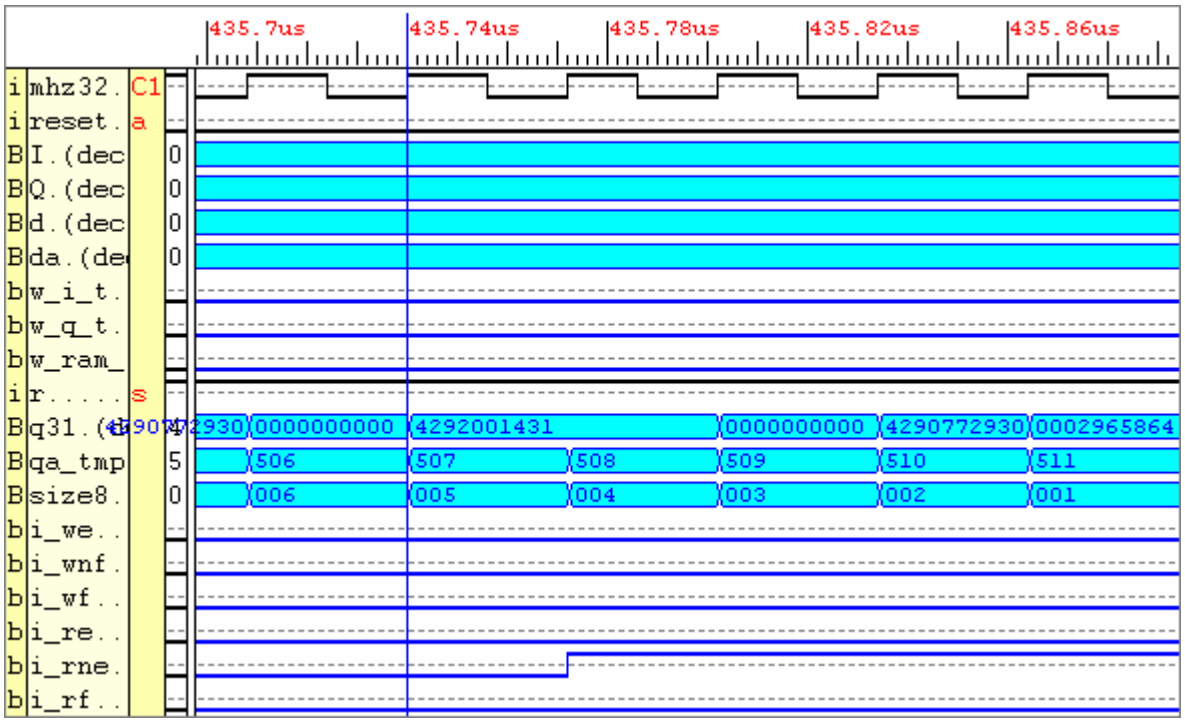


Figure A.11 End of Read Cycle Results for the Cross-Correlator, FIFO and FIFO Controller.

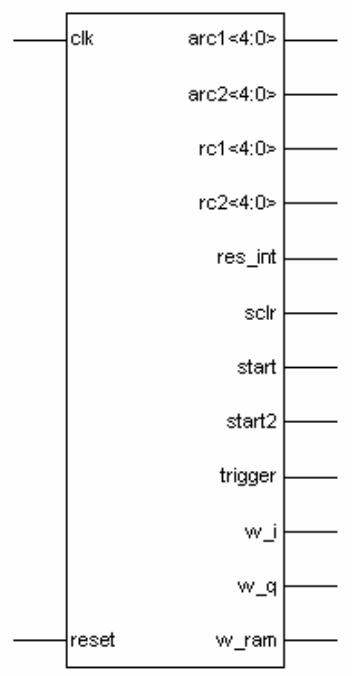


Figure A.12 Block Diagram for the Frequency and Phase Controller.

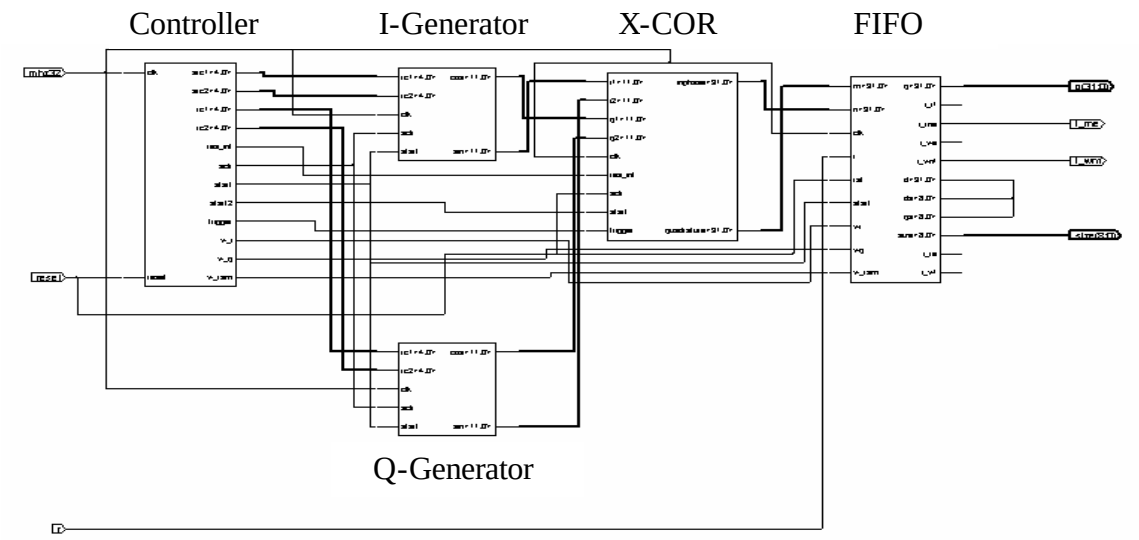


Figure A.13 Block Diagram for Controller, I & Q Generator, X-COR and FIFO.

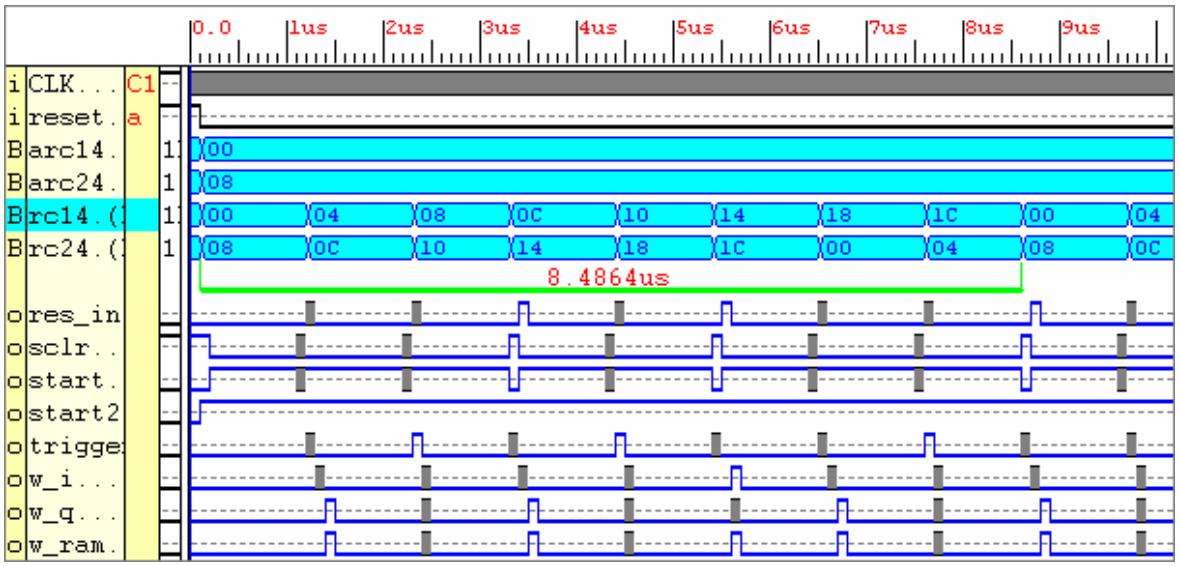


Figure A.14 Functional Simulation Results for the Frequency and Phase Controller.

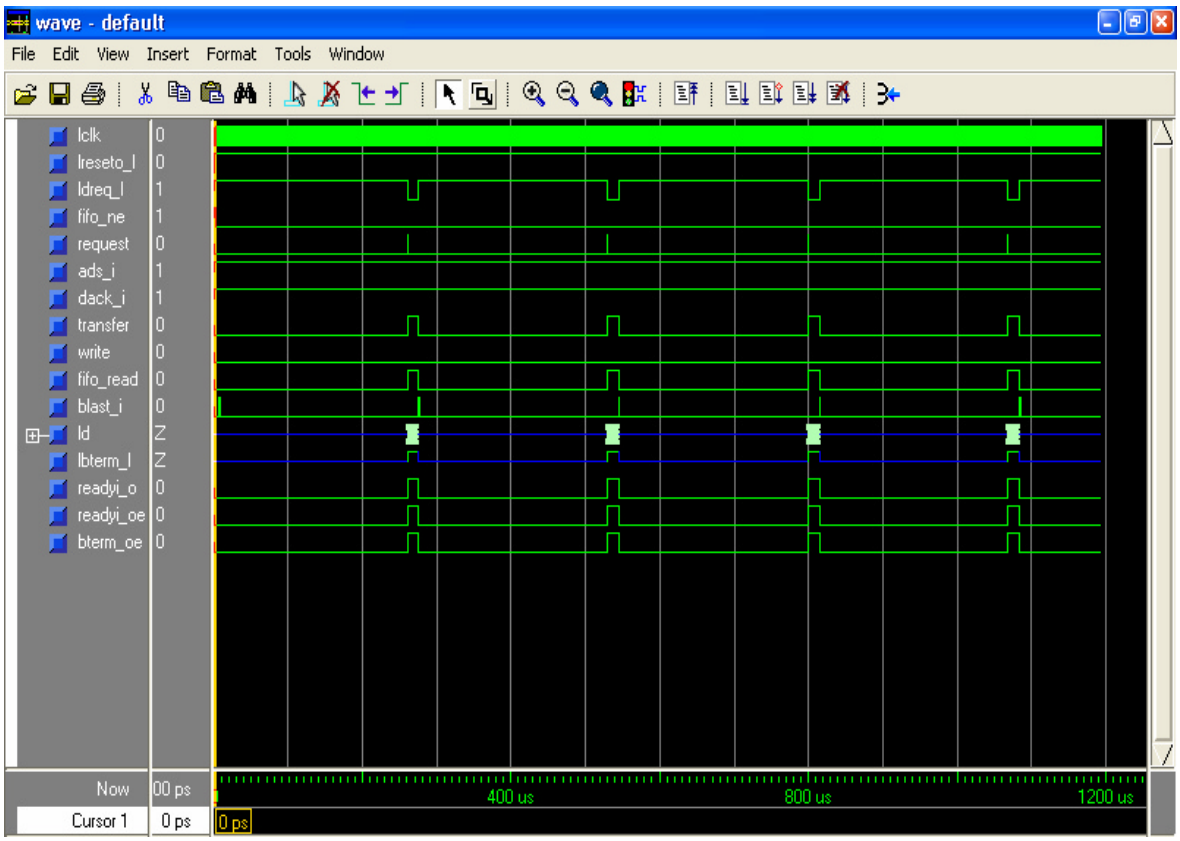


Figure A.15 Functional Simulation Results for the 8-Phase Auto-Switching Dual-Channel Correlator.

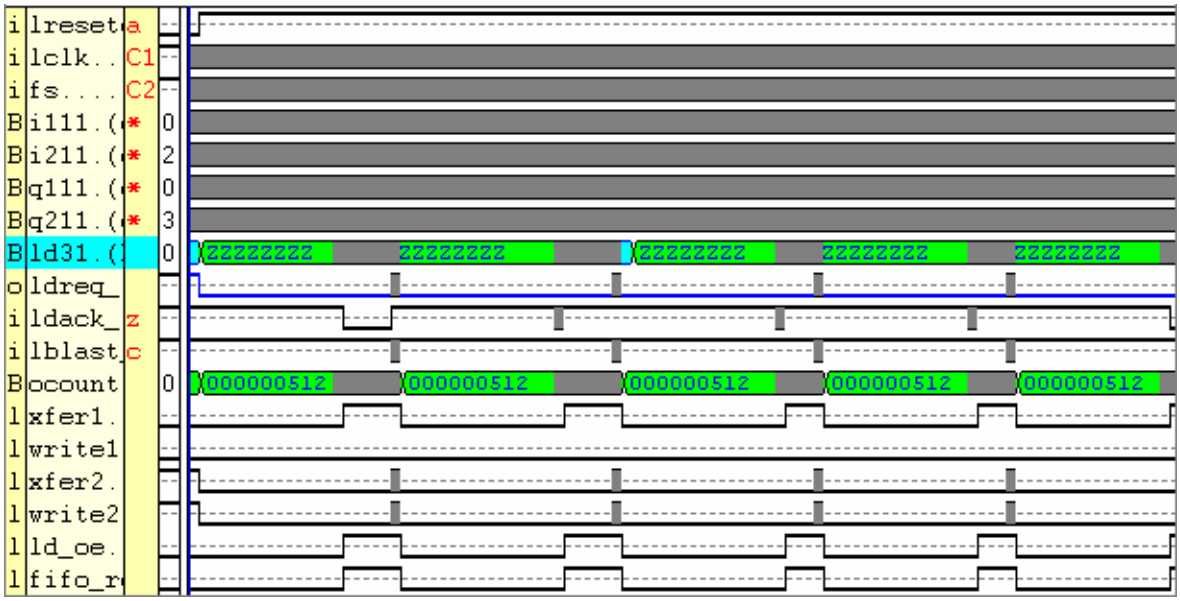


Figure A.16 Functional Simulation Results for the Dual-Channel Correlator System.

```
Design Summary
   Number of errors:      0    Number of warnings:   36
   Number of Slices:                   550 out of  33,792    1%
   Number of Slices containing unrelated logic:  0 out of     550    0%
   Number of Slice Flip Flops:         728 out of  67,584    1%
   Total Number 4 input LUTs:          695 out of  67,584    1%
      Number used as LUTs:                          678
      Number used as a route-thru:                   17
   Number of bonded IOBs:               51 out of     824    6%
      IOB Flip Flops:                                 1
   Number of Block RAMs:                 1 out of     144    1%
   Number of MULT18X18s:                 4 out of     144    2%
   Number of GCLKs:                      1 out of      16    6%
Total equivalent gate count for design:  92,867
Additional JTAG gate count for IOBs:  2,448
Design statistics:
   Minimum period:  10.825ns (Maximum frequency:  92.379MHz)
   Maximum path delay from/to any node:   6.724ns
   Maximum net delay:   9.837ns
   Minimum input arrival time before clock:   1.806ns
   Minimum output required time after clock:  13.276ns
```

Figure A.17 8-Phase Auto-Switching Dual-Channel Correlator Design Summary.

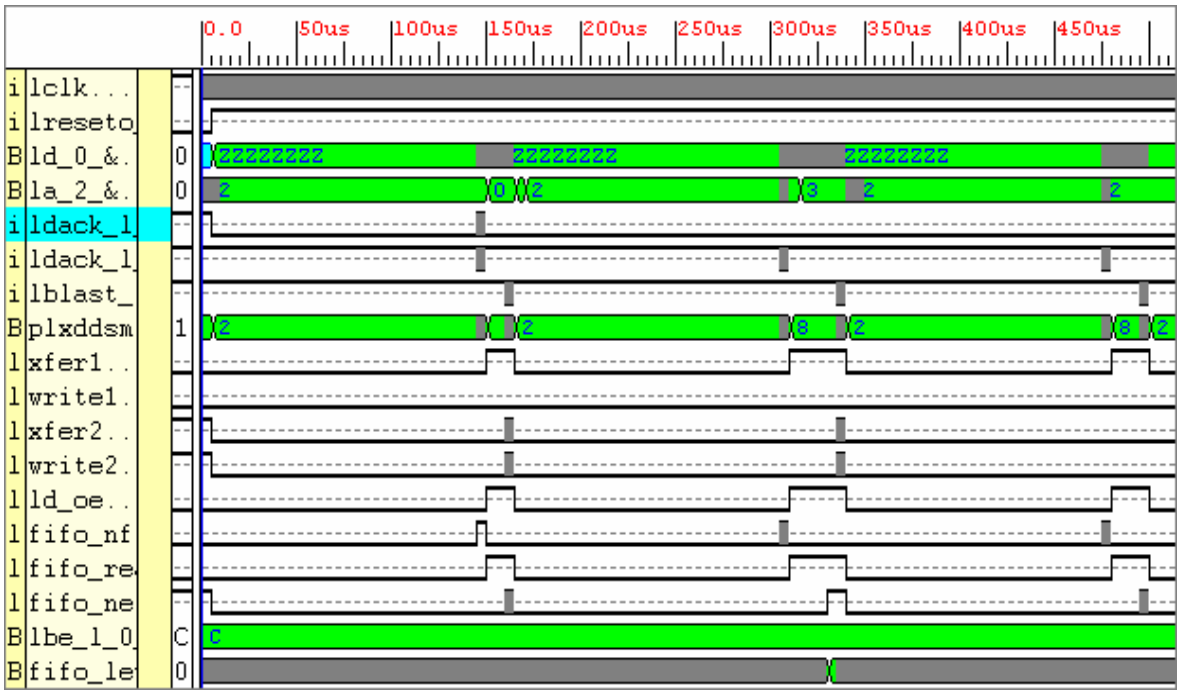


Figure A.18 Timing Simulation Results for the 8-Phase Dual-Channel Correlator System.

```
Design Summary
   Number of errors:      0
   Number of warnings:   36
   Number of Slices:                   443 out of  33,792    1%
   Number of Slices containing
      unrelated logic:                   0 out of     443    0%
   Number of Slice Flip Flops:         622 out of  67,584    1%
   Total Number 4 input LUTs:          495 out of  67,584    1%
      Number used as LUTs:                        469
      Number used as a route-thru:                 26
   Number of bonded IOBs:               99 out of     824   12%
      IOB Flip Flops:                               1
   Number of Block RAMs:                1 out of     144    1%
   Number of MULT18X18s:                4 out of     144    2%
   Number of GCLKs:                     1 out of      16    6%
Total equivalent gate count for design:  90,723
Additional JTAG gate count for IOBs:  4,752
Design statistics:
   Minimum period:  12.397ns (Maximum frequency:  80.665MHz)
   Maximum path delay from/to any node:   7.234ns
   Maximum net delay:   8.572ns
   Minimum input arrival time before clock:  10.262ns
   Minimum output required time after clock:  11.644ns
```

Figure A.19 8-Phase Auto-Switching Dual-Channel Correlator Design Summary.

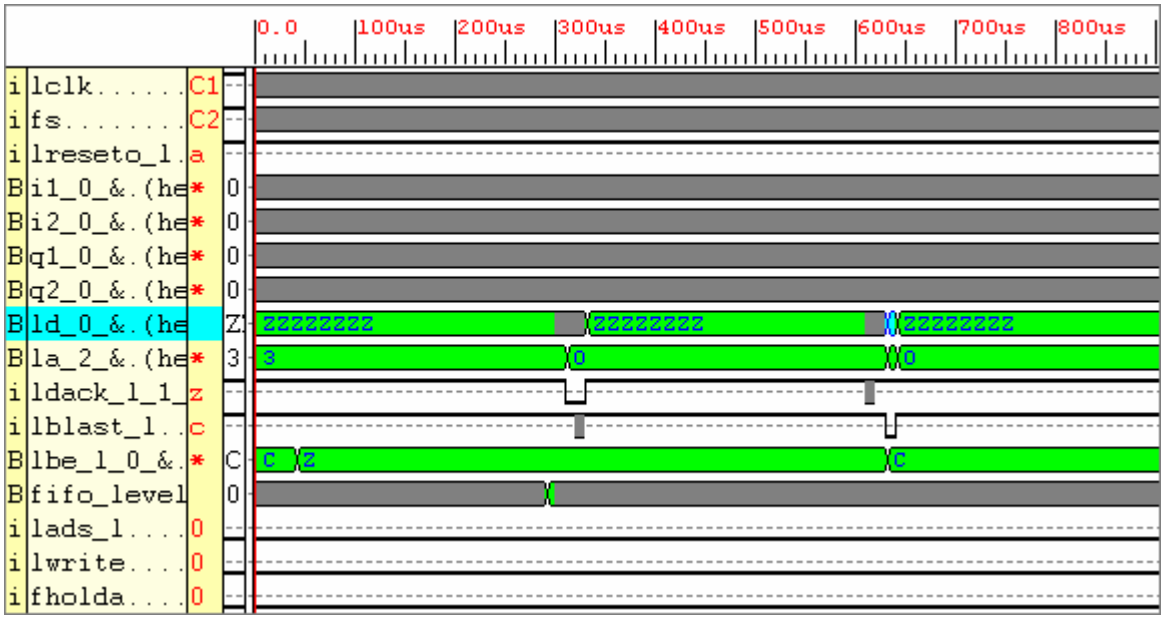


Figure A.20 Timing Simulation Results for the Dual-Channel Correlator System.

Appendix B Crossed-Dipole Antenna Modelling

The antenna modelled in Mininec is a crossed-dipole with right-handed circular polarisation tuned to 38.2 MHz. Circular polarisation is a special case of elliptical polarisation. The cross-dipole has the advantage of being double polarised, in the sense that both the vertical and horizontal directions of the incoming wavefront are measured. This is possible because the propagating electric and magnetic fields can have two orthogonal components with independent amplitudes and phases, while the frequency is the same. In Radio Astronomy right-handed polarisation refers to the direction of the electric field's vector rotation as observed by the receiver. The radiation pattern of the crossed-dipole is formulated in [119]:

$$F(\theta,\varphi) = \frac{\cos[\frac{1}{2}\pi|\sin(\theta)|\sin(\varphi)]\sin[\frac{1}{2}\pi\cos(\varphi)]}{\sqrt{1-\sin^2(\theta)\sin^2(\varphi)}} \qquad \text{(B-1)}$$

In equation (B-1), θ is the zenith angle and f is azimuth angle using spherical coordinates. The antenna consists of two resonant dipoles perpendicular to each other in Fig. B.1. An inductor is connected across each dipole centre terminal to nullify the imaginary capacitive reactance part of the the total impedance at resonance. The dipole's real impedance matching is achieved by connecting one transformer to each dipole's electrical centre.

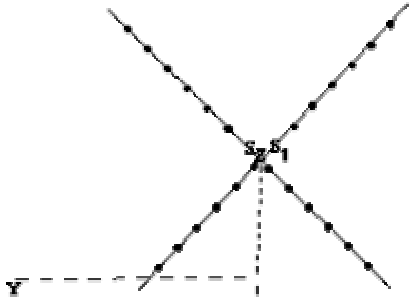


Figure B.1 Crossed-Dipole Antenna Modelling.

A 90-degree phasing line of 72-Ohm coaxial cable is inserted at the matched transformer output. The 90-degree phasing of the two dipoles is crucial in obtaining an omni-directional pattern. The phasing line length depends on the velocity factor of the coaxial cable. 72 Ohm coaxial cable has either solid or foam insulation. The solid and foam insulations have a velocity factor of 0.66 and 0.78, respectively.

The two signals are routed through a power combiner. The output is fed to the main 50R feed-line leading to the PA. The antenna board schematic is in Fig. B.2.

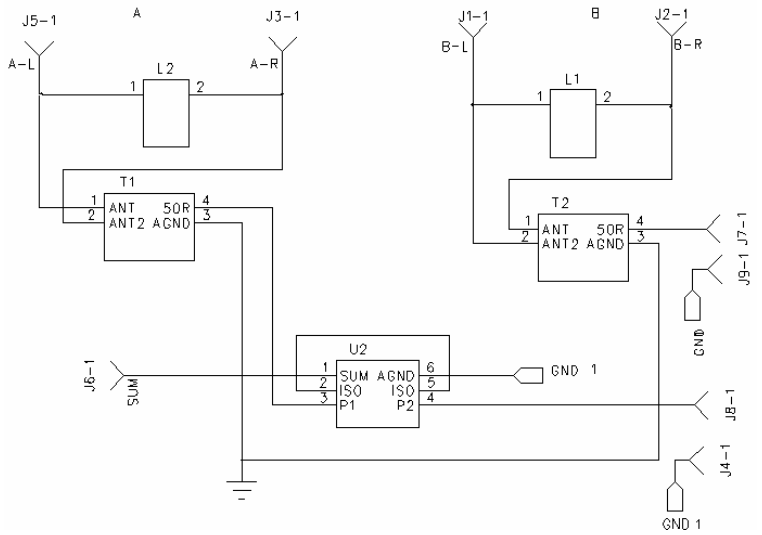


Figure B.2 Crossed-Dipole Antenna PCB Schematic.

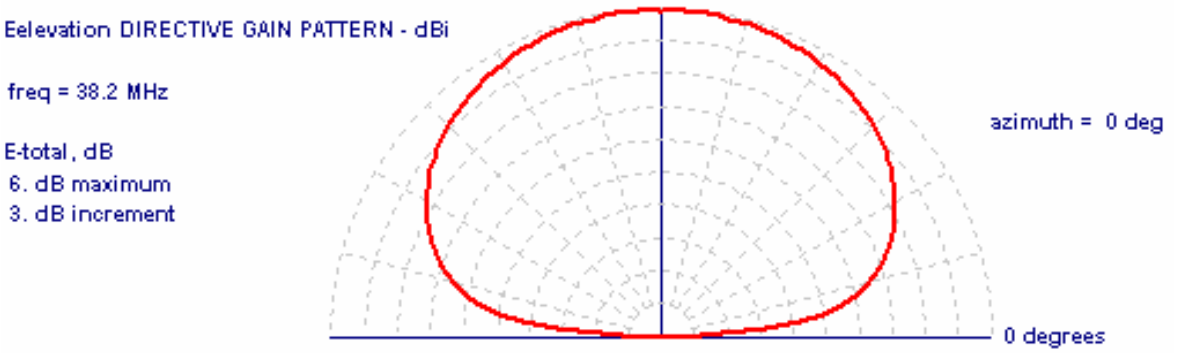


Figure B.3 Crossed-Dipole Vertical Pattern.

The antenna is quarter wavelengths above ground. Non-resonant guy wires of length close to 140 cm could support it, depending on the construction of the mast. Resonant guy wires act as antennas. They radiate the signal or its harmonics providing a significant source of RF losses. The ground is modelled with a dielectric constant of 15 and conductivity of 0.0278 S/m. Its 3-D construction model is in Fig. B.1. Mininec visualises the antenna structure only and not the ground plane.

From the normalised vertical radiation pattern of Fig. B.3, the maximum gain is 5.8 dBi at 90 deg elevation angle. Gain is constant for all azimuth angles. The HPBW is 83.36 deg. The horizontal pattern at maximum gain elevation angle is in Fig. B.4.

The model is compared against ITU conforming cross-dipole antennas, such as the HX 950 model from HFBC [120]. The results agree to the commercial models. The horizontal and elevation patterns of the HX950 crossed dipoles are in Fig. B.5.

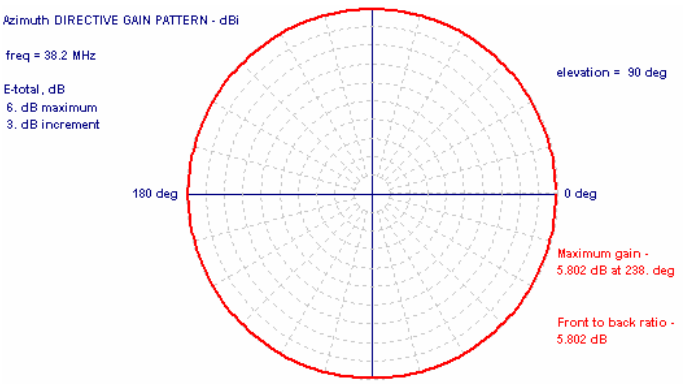


Figure B.4 Crossed-Dipole Horizontal Pattern Maximum Gain Elevation.

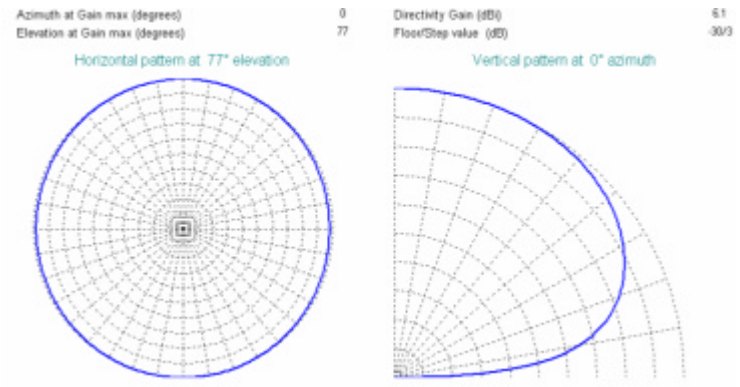


Figure B.5 HX950 Horizontal and Elevation Patterns.

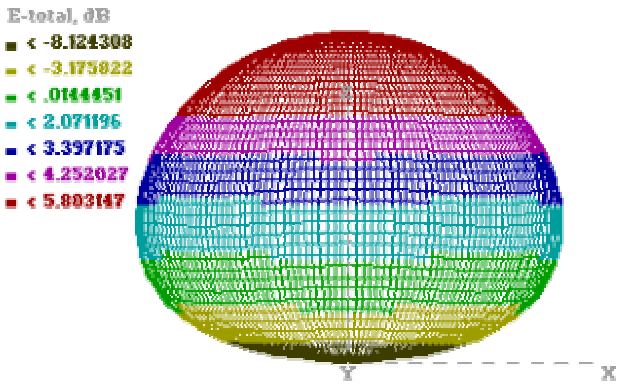


Figure B.6 3-D Crossed Dipole Radiation Pattern.

The 3-D radiation pattern of the crossed dipole is in Fig. B.6. The red area corresponds to the maximum gain of 5.8 dB in the zenith direction.

Appendix C Priamos RF Receiver Unit

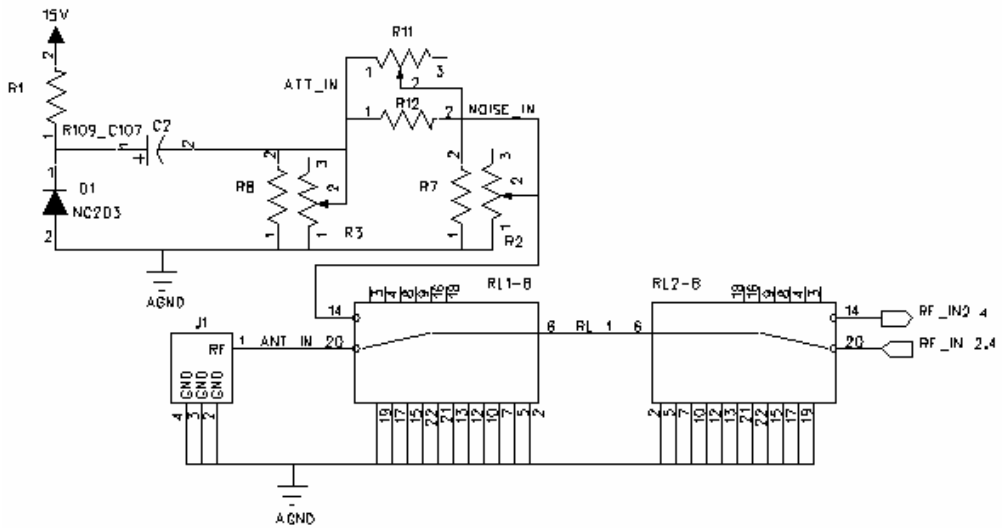


Figure C.1 RF Input, Switching and Calibration Schematic.

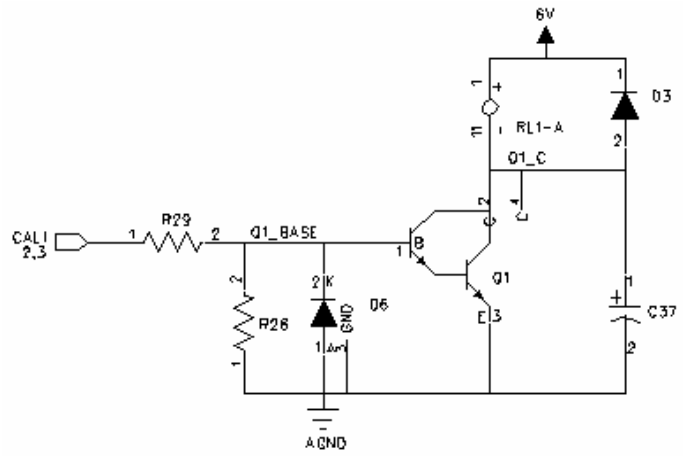


Figure C.2 RF Relays' Control Schematic.

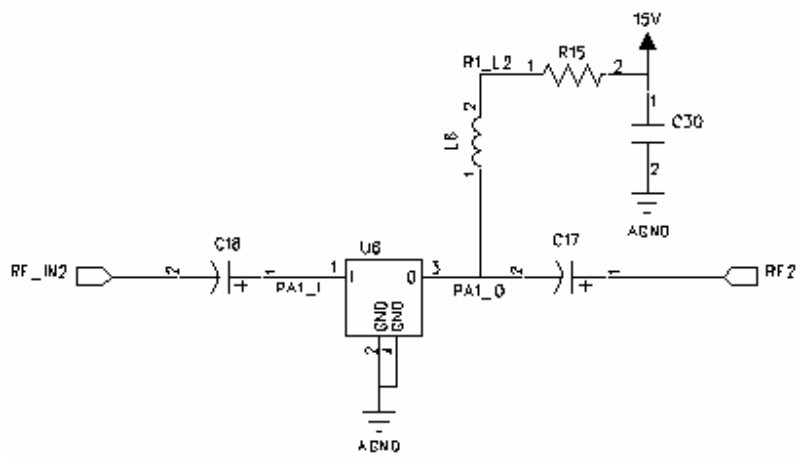


Figure C.3 PA Schematic.

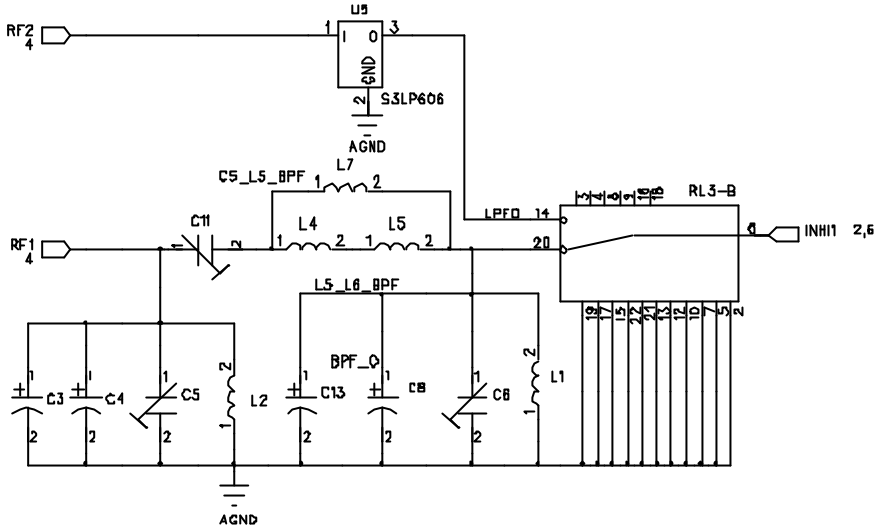


Figure C.4 BPF and LPF Schematic.

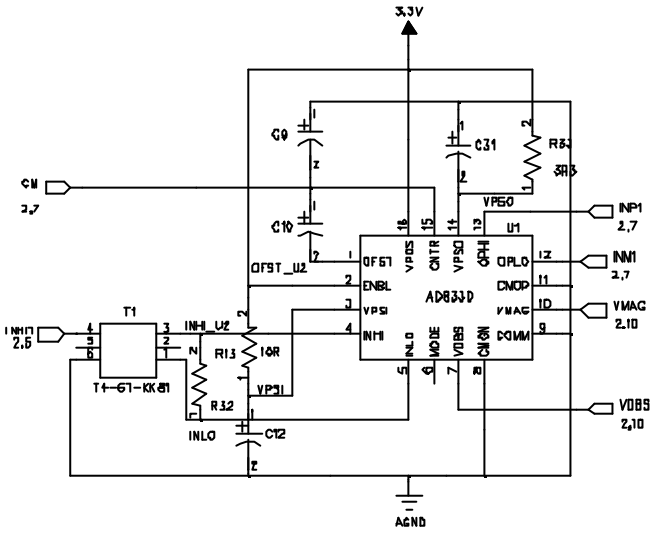


Figure C.5 AGC Schematic.

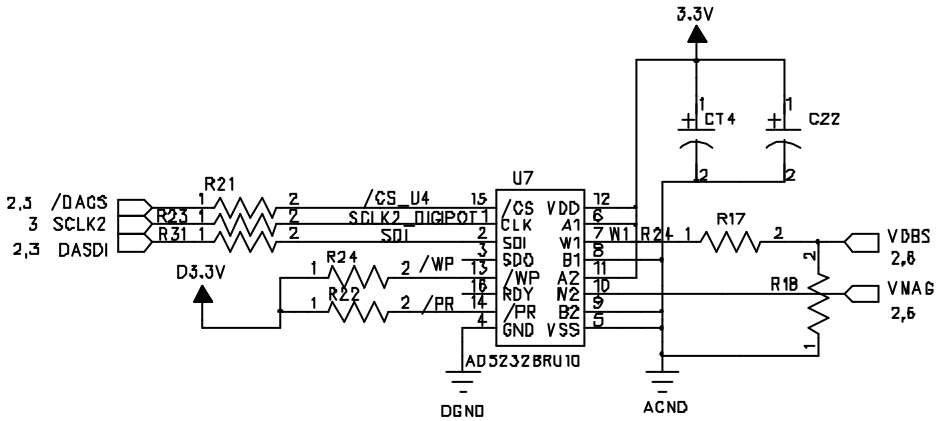


Figure C.6 Digital Potentiometer Schematic.

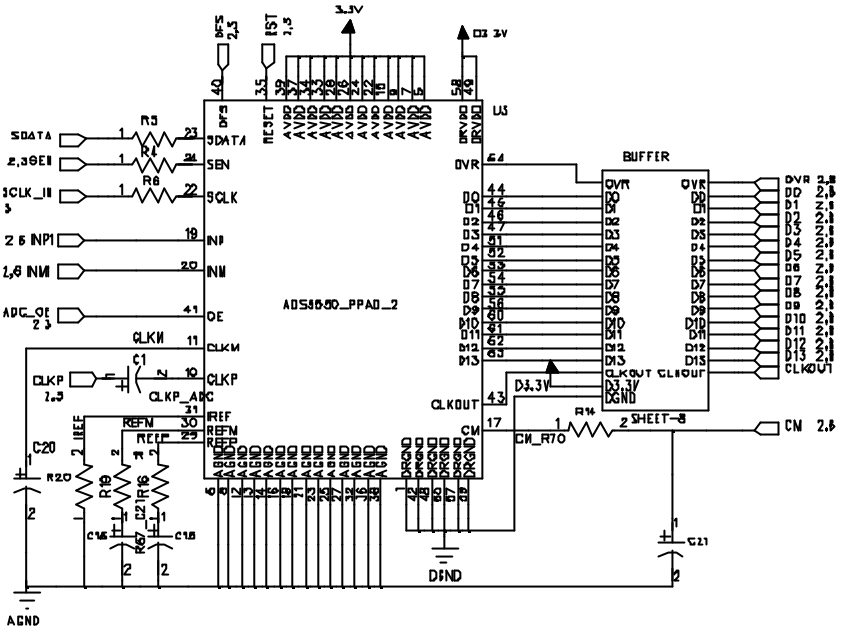
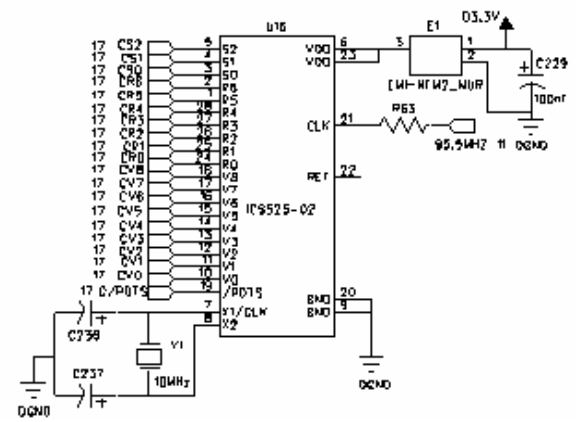
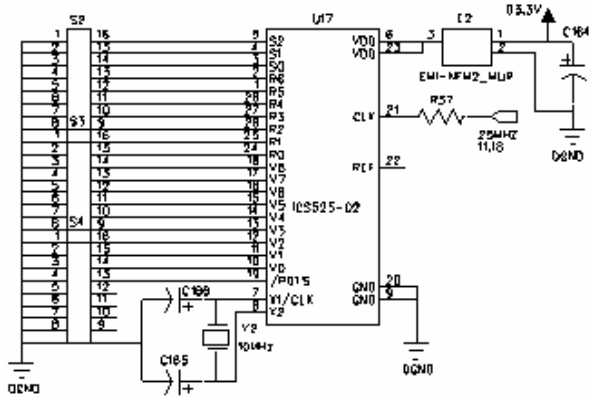


Figure C.7 ADC Schematic.



(a)



(b)

Figure C.8 Master Oscillator Schematic (a) & (b).

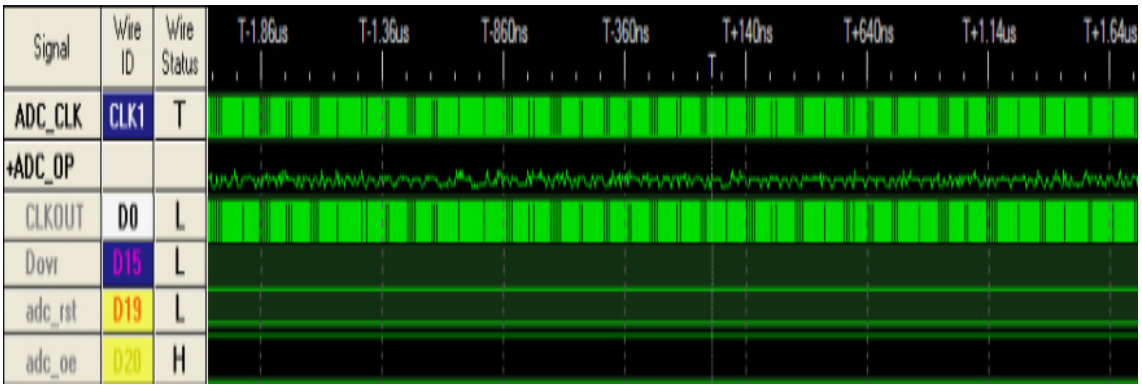


Figure C.9 ADC BPF Output.

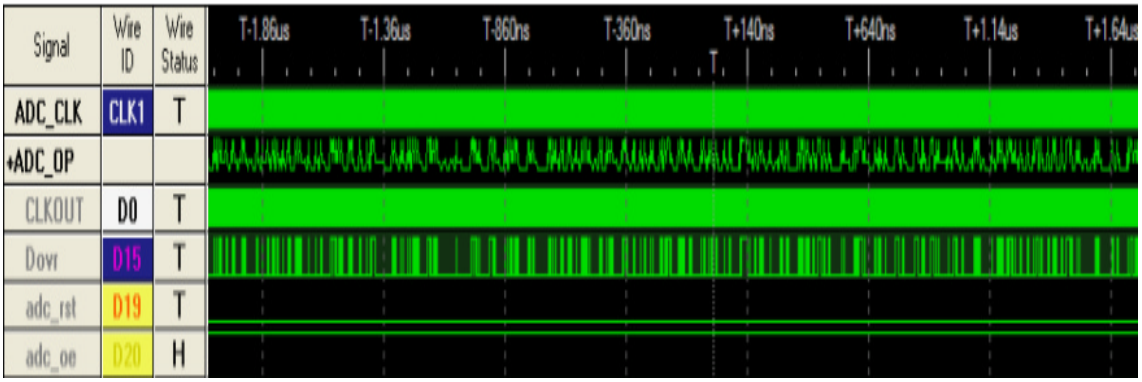


Figure C.10 ADC Output during Saturation.

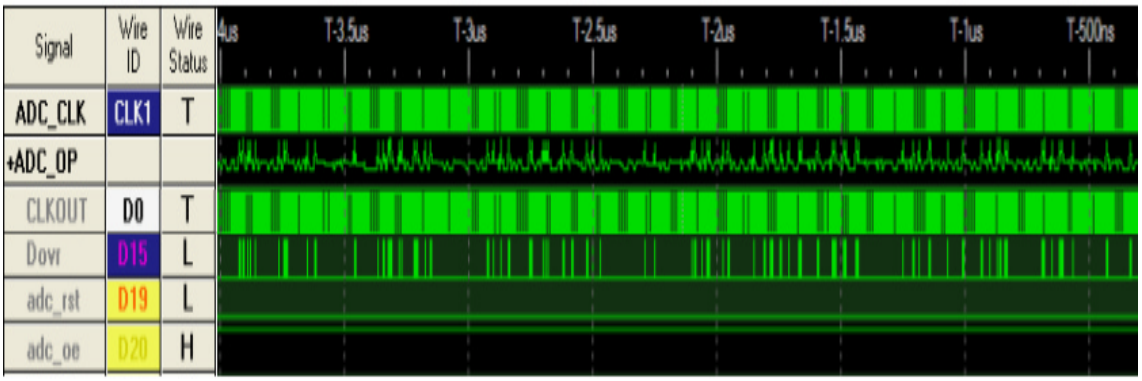


Figure C.11 Auto-Recovery from Saturation.

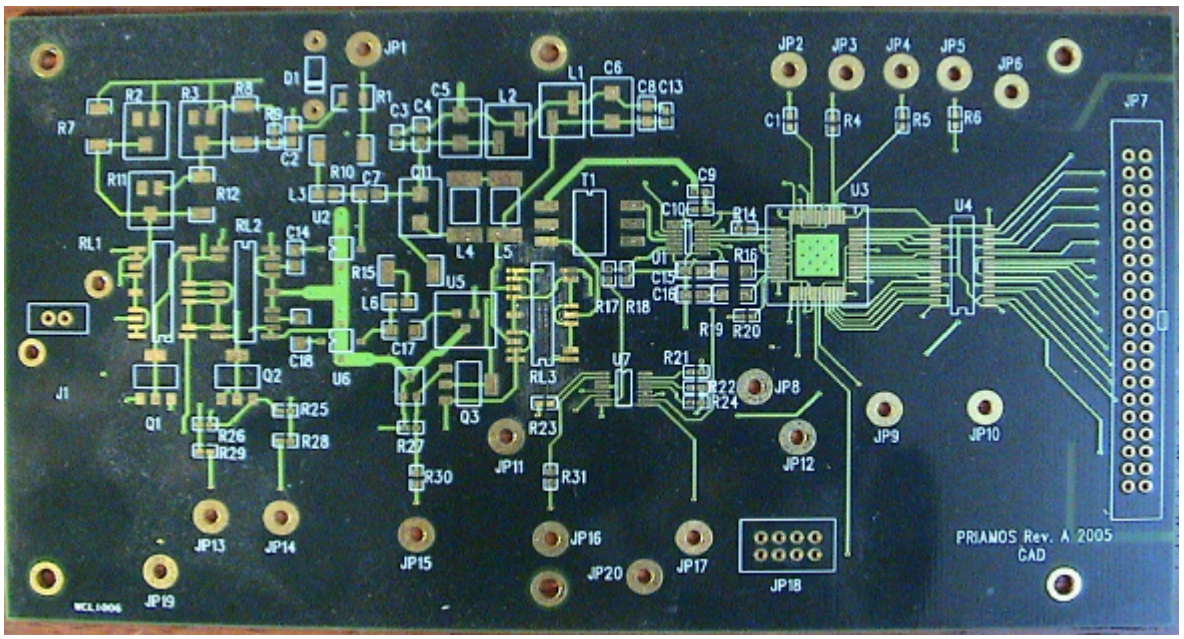


Figure C.12 4-Layer Priamos Antenna PCB Top-Side.

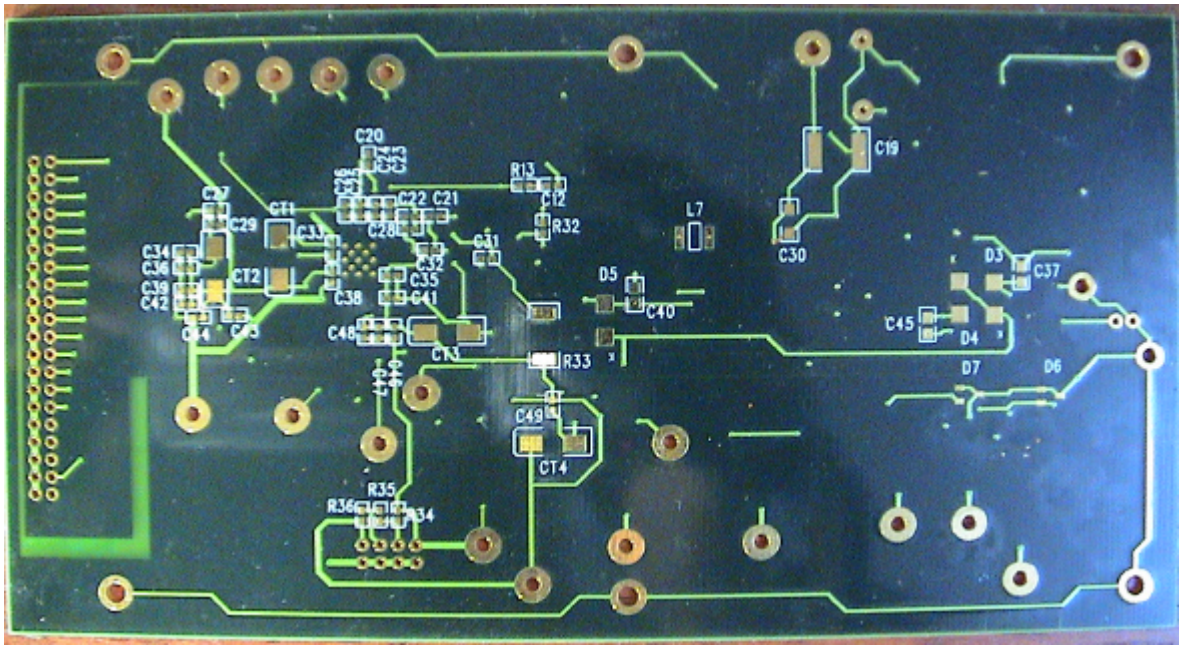


Figure C.13 4-Layer Priamos Antenna PCB Bottom-Side.

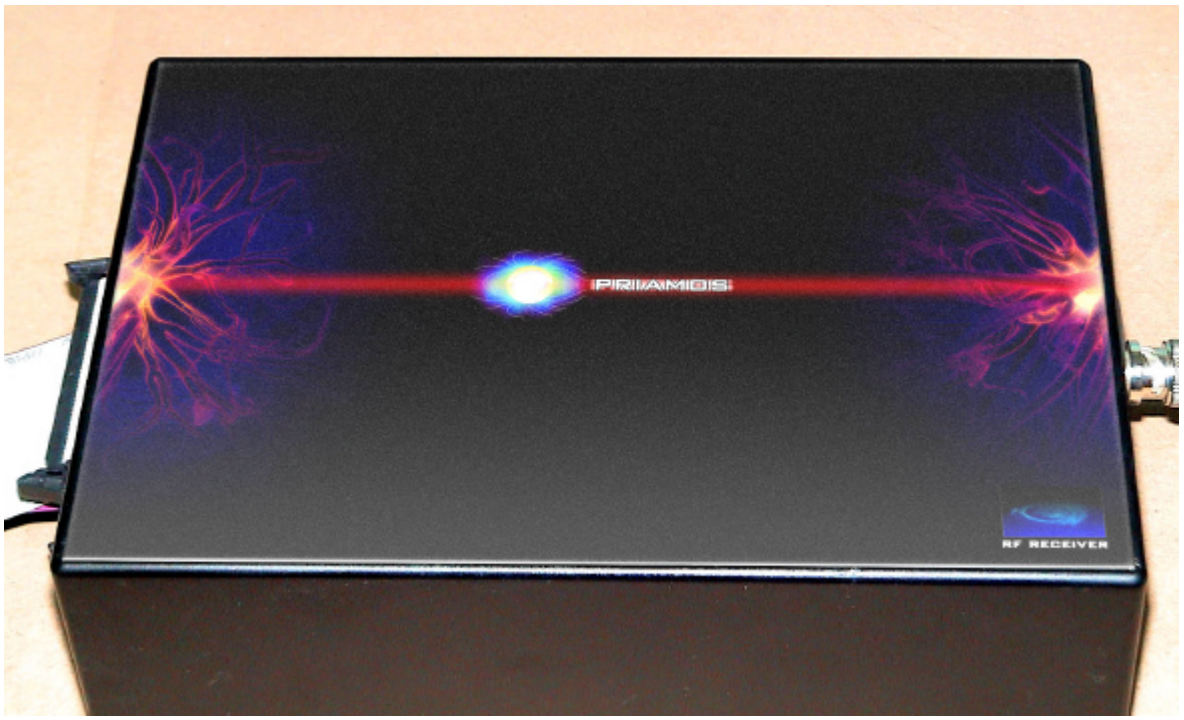


Figure C.14 Priamos RF Receiver Unit.

Appendix D Priamos DSP Engine

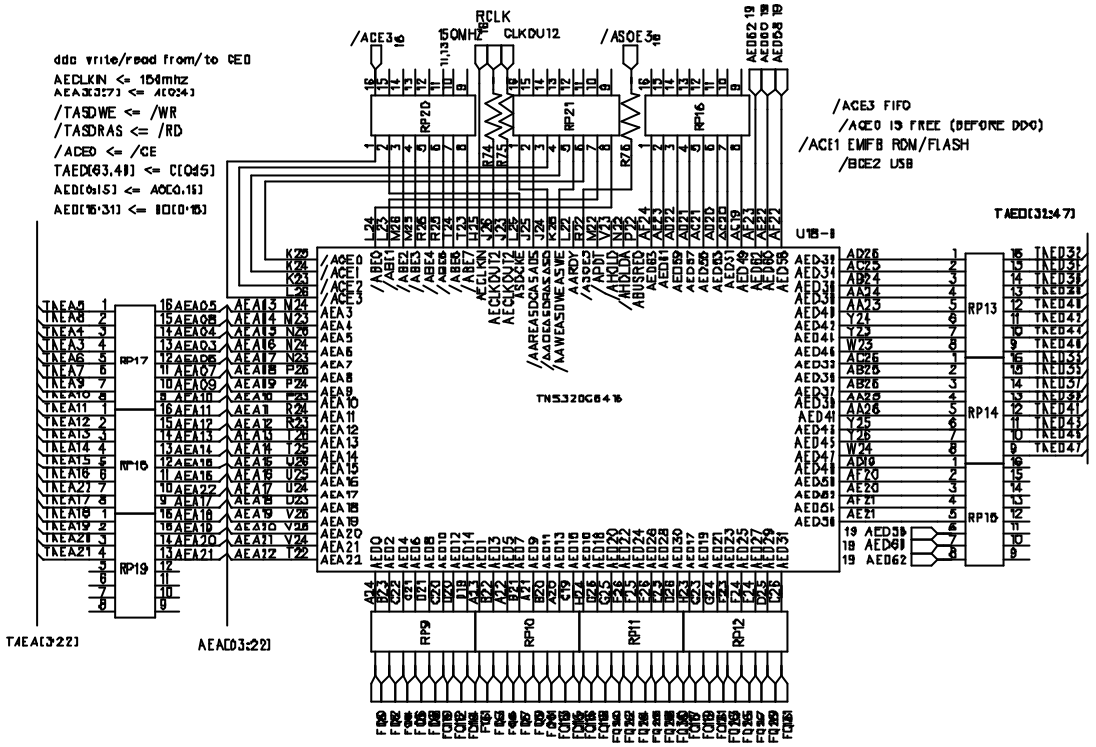


Figure D.1 DSP EMIF A Schematic.

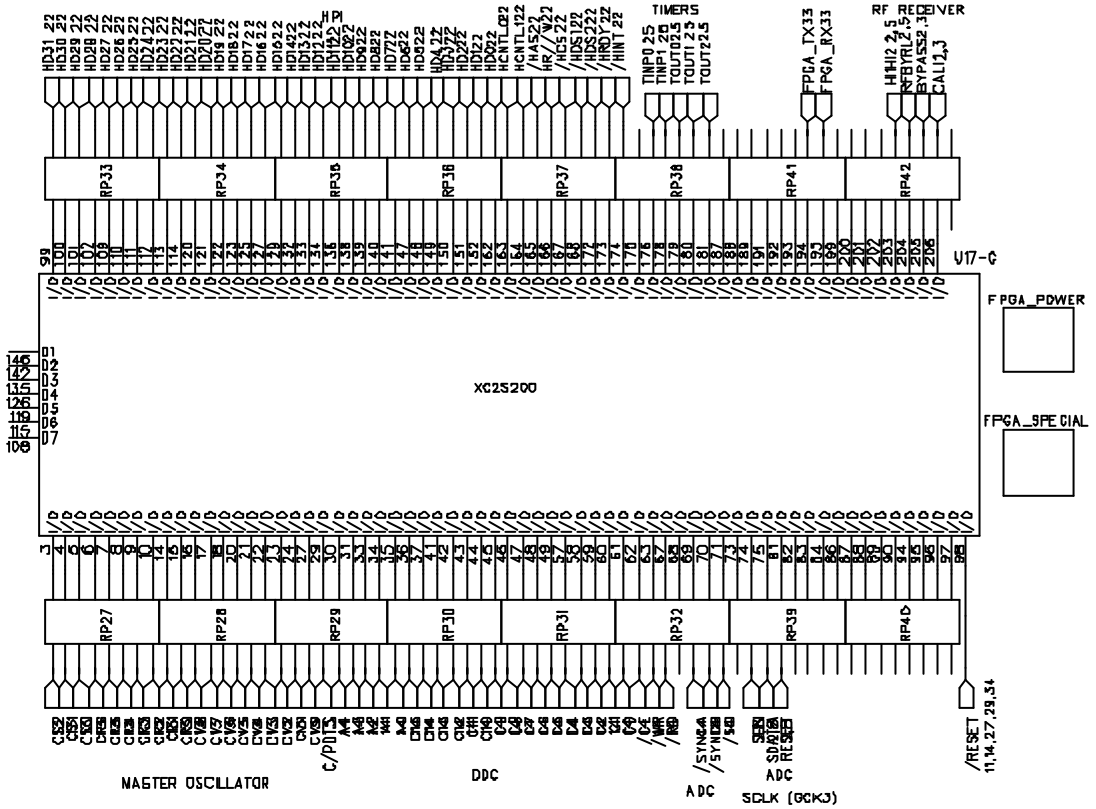


Figure D.2 FPGA Co-Processor.

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4. Preamplifier Design
5. RF Switching, Low Pass & Bandpass Filters Design
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7. Automatic Gain Controller Design
8. Analogue-to-Digital Converter Design
9. ADC Buffer Design
10. ADC Decoupling Circuit Design
11. DSP Board Top Level Design
12. DDC Buffer Design
13. Master Oscillator Design
14. Direct Digital Converter Design
15. DDC Decoupling Design
16. DSP Fifo Design
17. FIFO Decoupling Circuit Design
18. DSP Partial Top Level Design
19. EMIFA Design
20. EMIFB Design
21. McBSP1 & UTOPIA Design
22. HPI/McBSP2/GPIO Design
23. C6416 Power Supply & Decoupling Circuit
24. DSP Flash Memory Design
25. DSP UART Design
26. GPS Programming & DSP Interface
27. EMU/JTAG/Controller/GPIO Design
28. Digital-to-Analogue Converter Design
29. USB Controller Design
30. FPGA I/O
31. FPGA Special & Flash Design
32. FPGA Power Supply & Decoupling Circuit Design
33. FPGA UART
34. Power Supply Design

(a)

SCHEMATIC CONTENTS

1. Notes and Contents
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14. Direct Digital Converter Design
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16. GPS Programming & FPGA Interface
17. FPGA I/O
18. FPGA Special & Flash Design
19. FPGA Power Supply & Decoupling Circuit Design
20. FPGA UART
21. USB Controller Design
22. Power Supply Design

(b)

Figure D.3 (a) DSP- (b) FPGA-Based Schematic Contents.

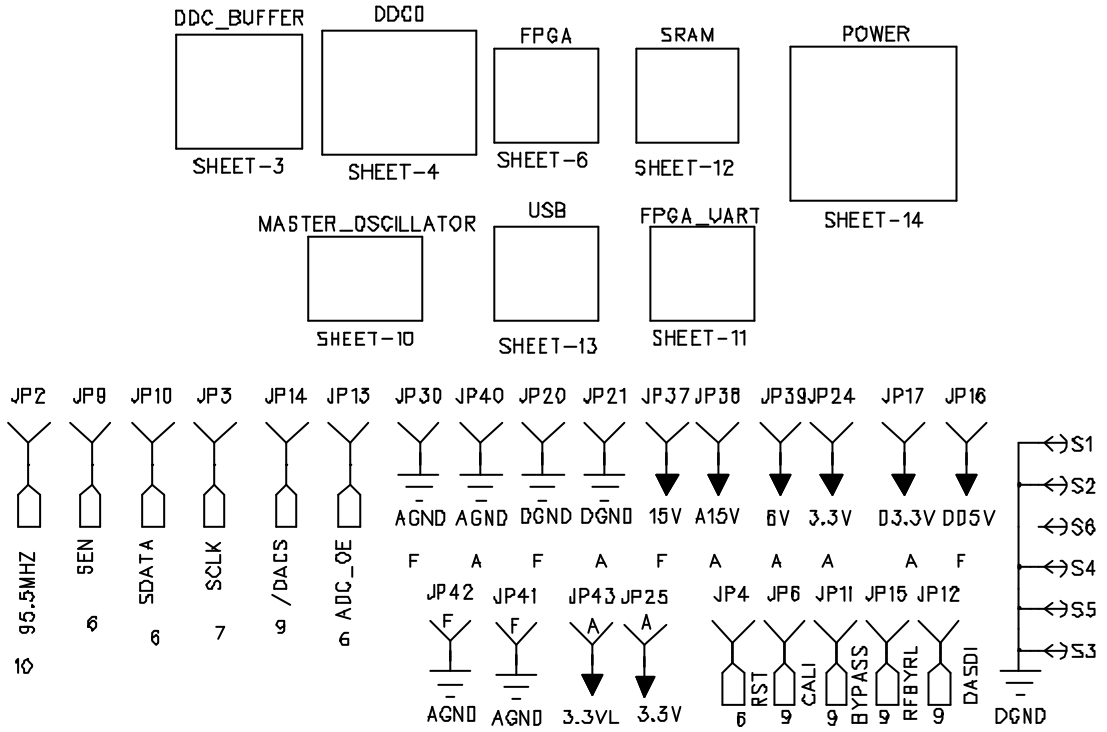

Figure D.4 Priamos DSP Engine Board Top-Level Schematic.

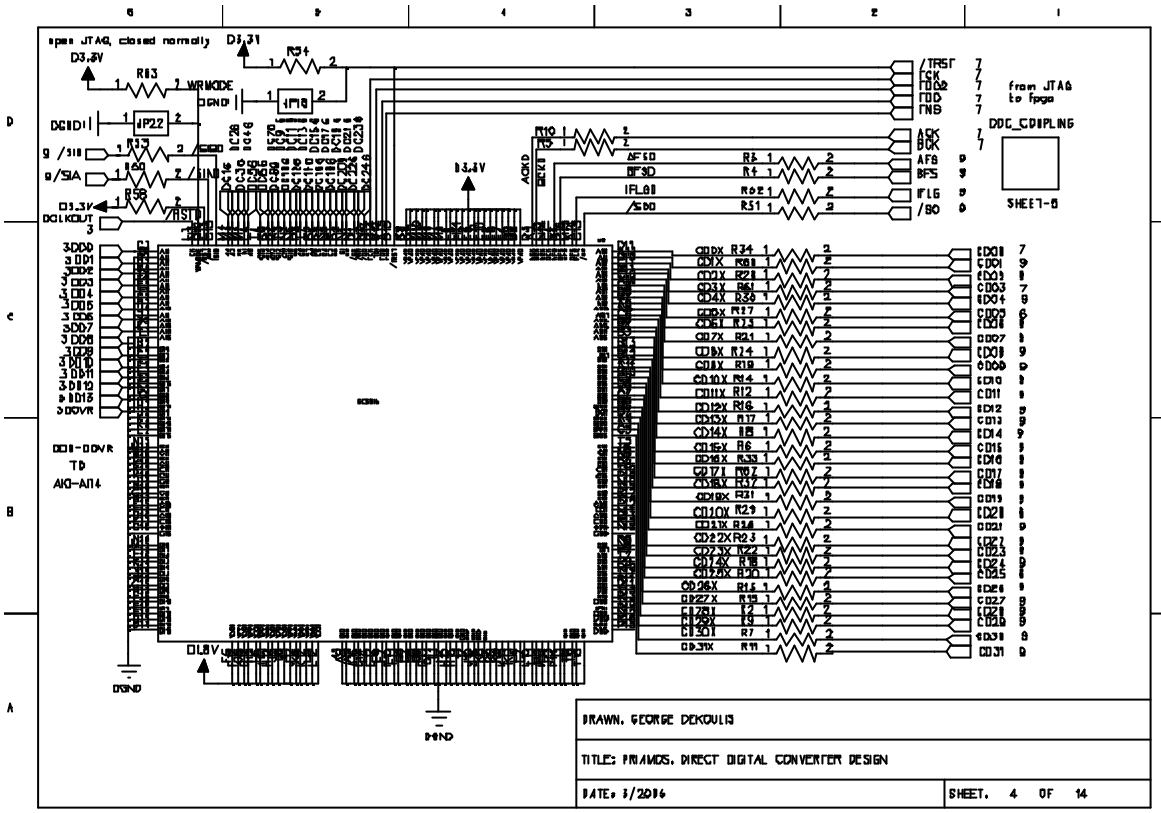

Figure D.5 DDC Circuit Schematic.

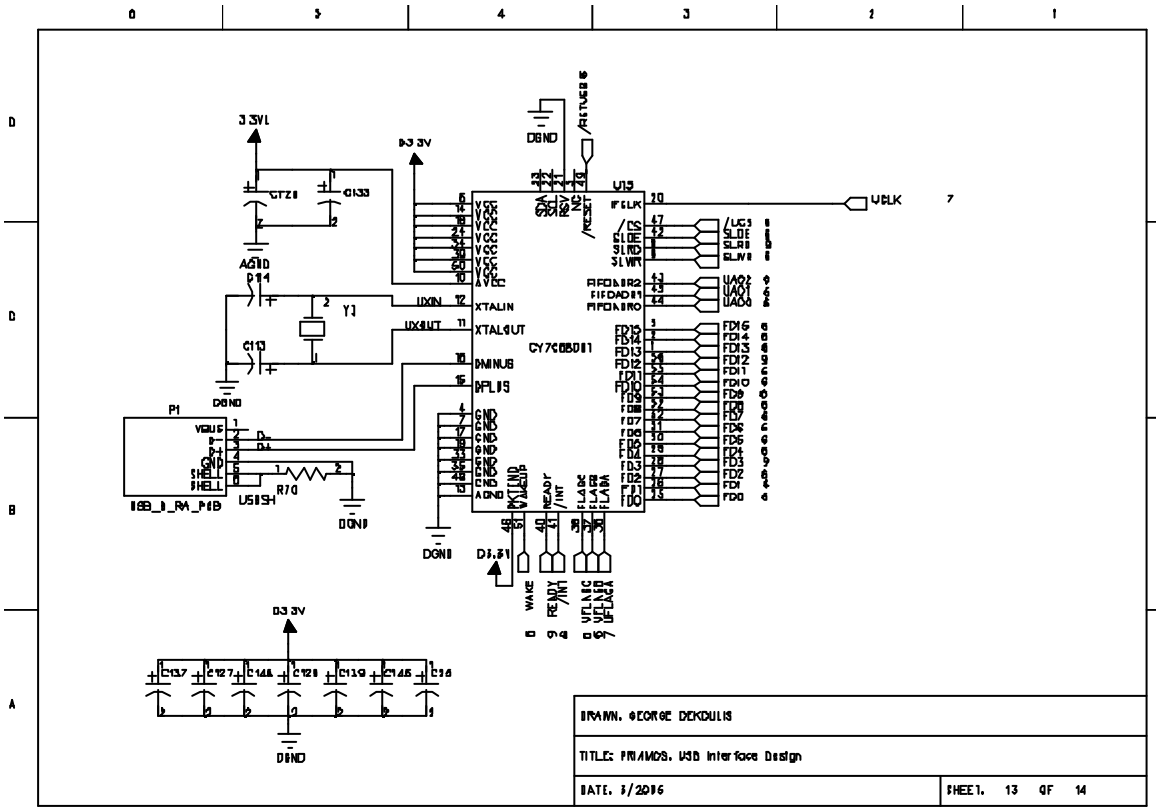

Figure D.6 USB 2.0 Interface Schematic.

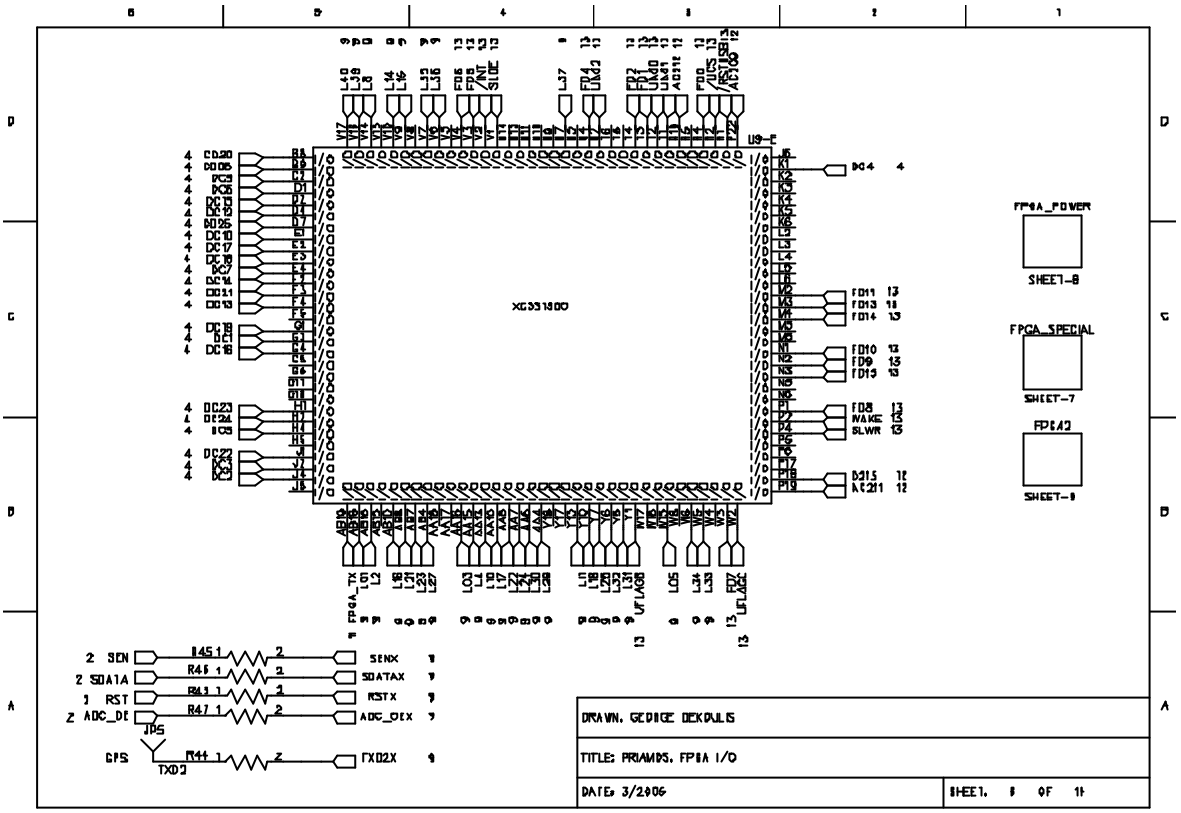

Figure D.7 FPGA I/O Circuit Schematic 1.

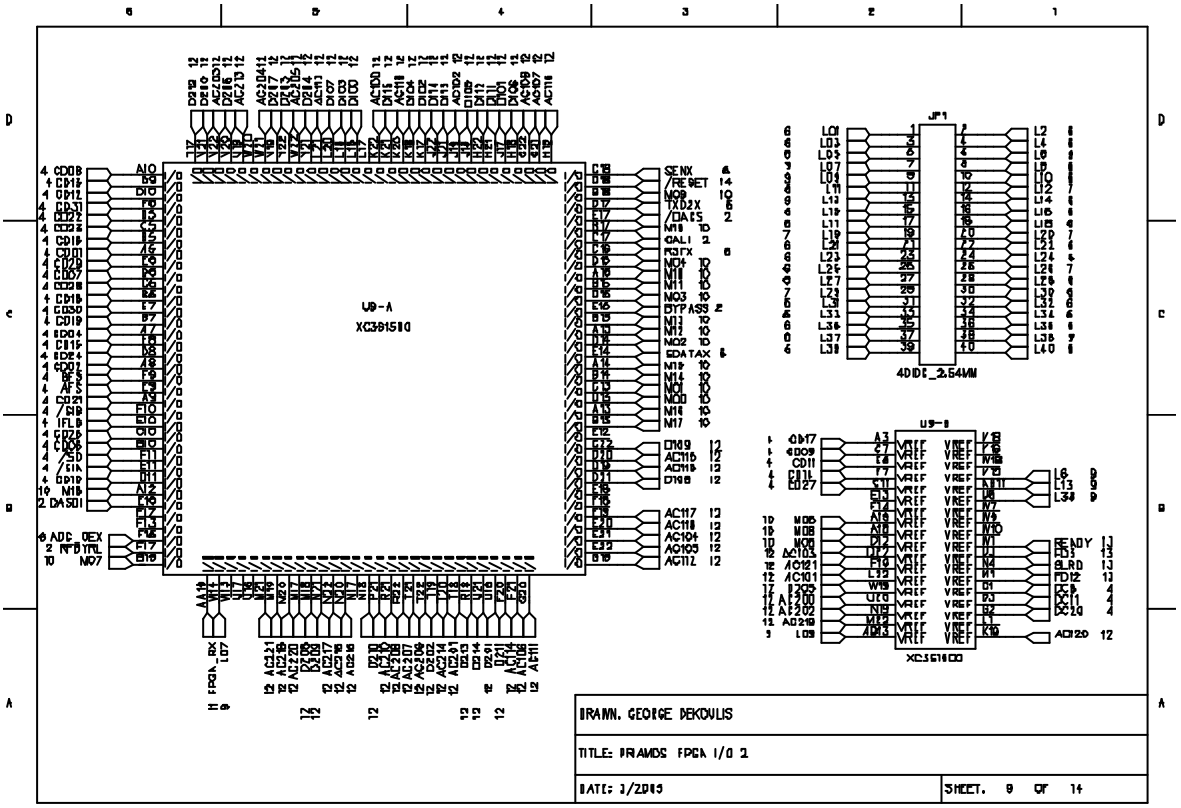

Figure D.8 FPGA I/O Circuit Schematic 2.

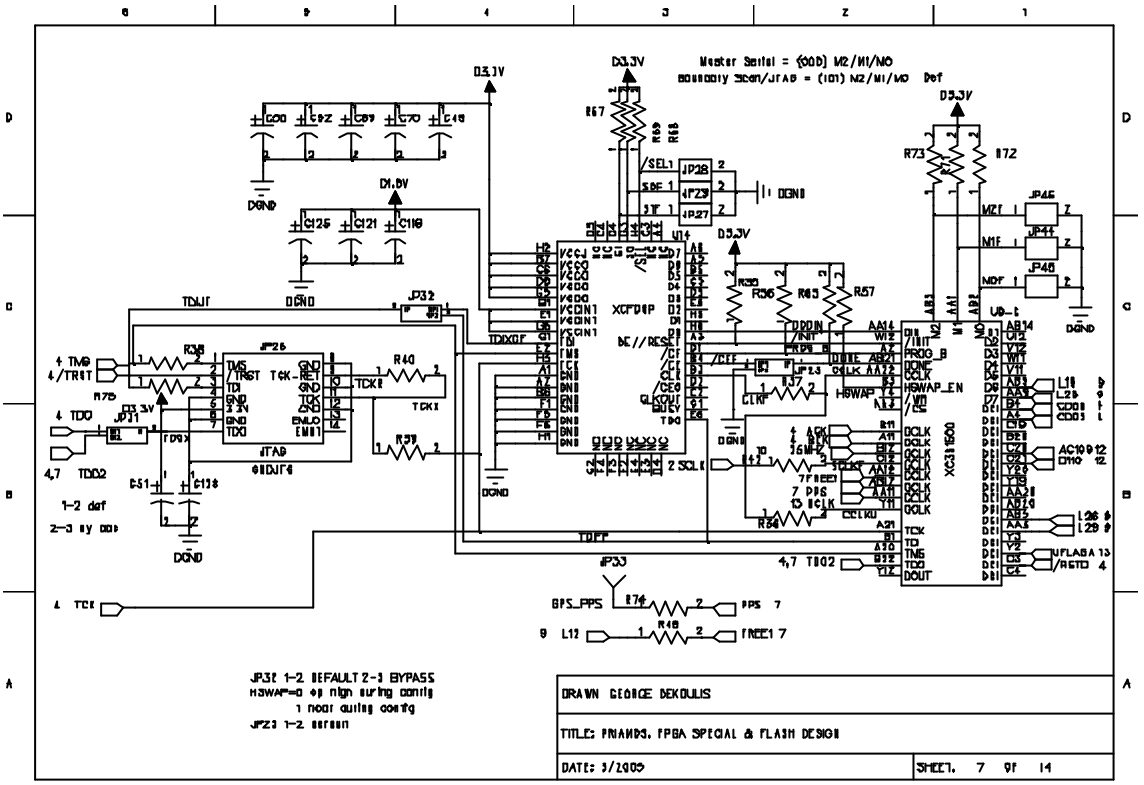

Figure D.9 FPGA Programming and Special I/O Circuit Schematic.

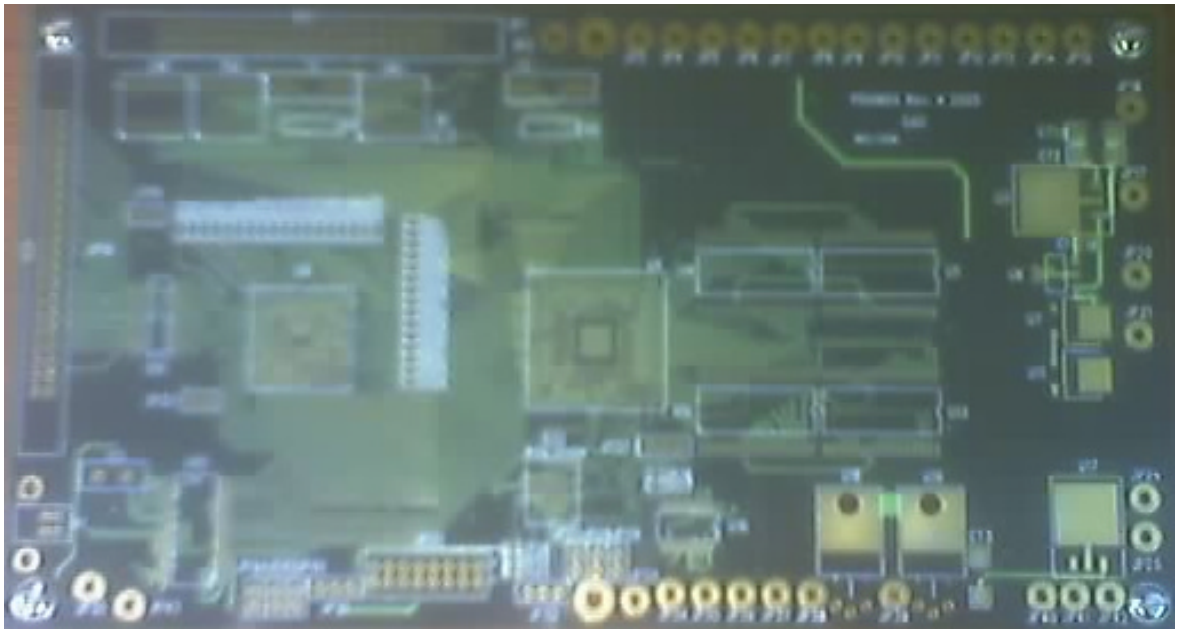

Figure D.10 6-Layer Priamos DSP Engine PCB Top-Side.

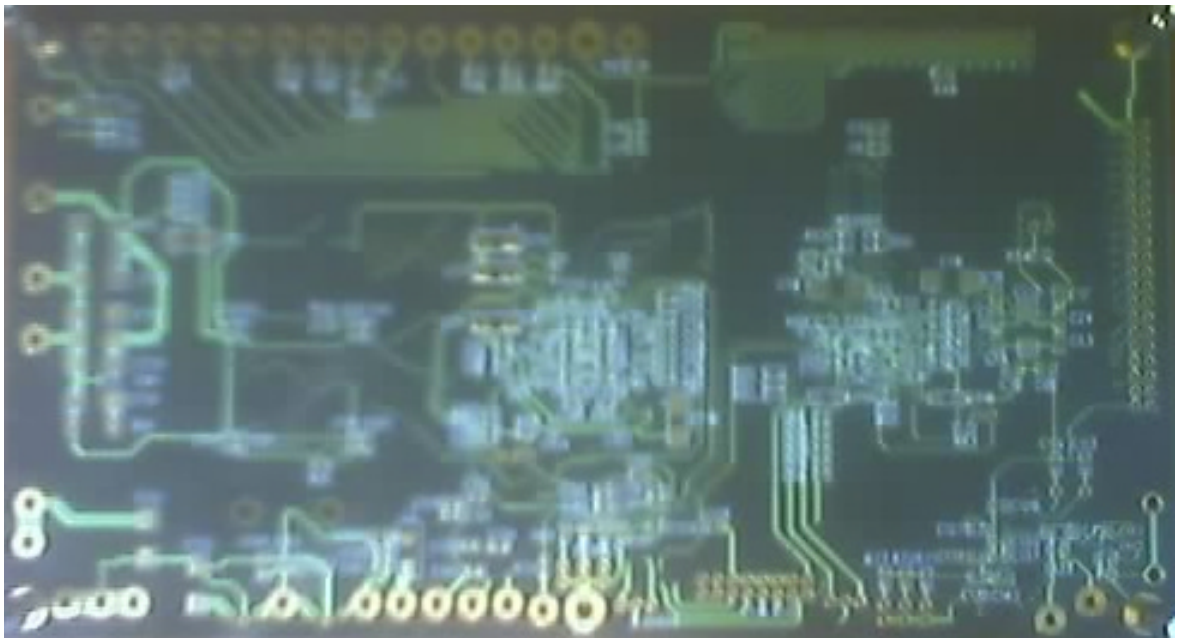

Figure D.11 6-Layer Priamos DSP Engine PCB Bottom-Side.

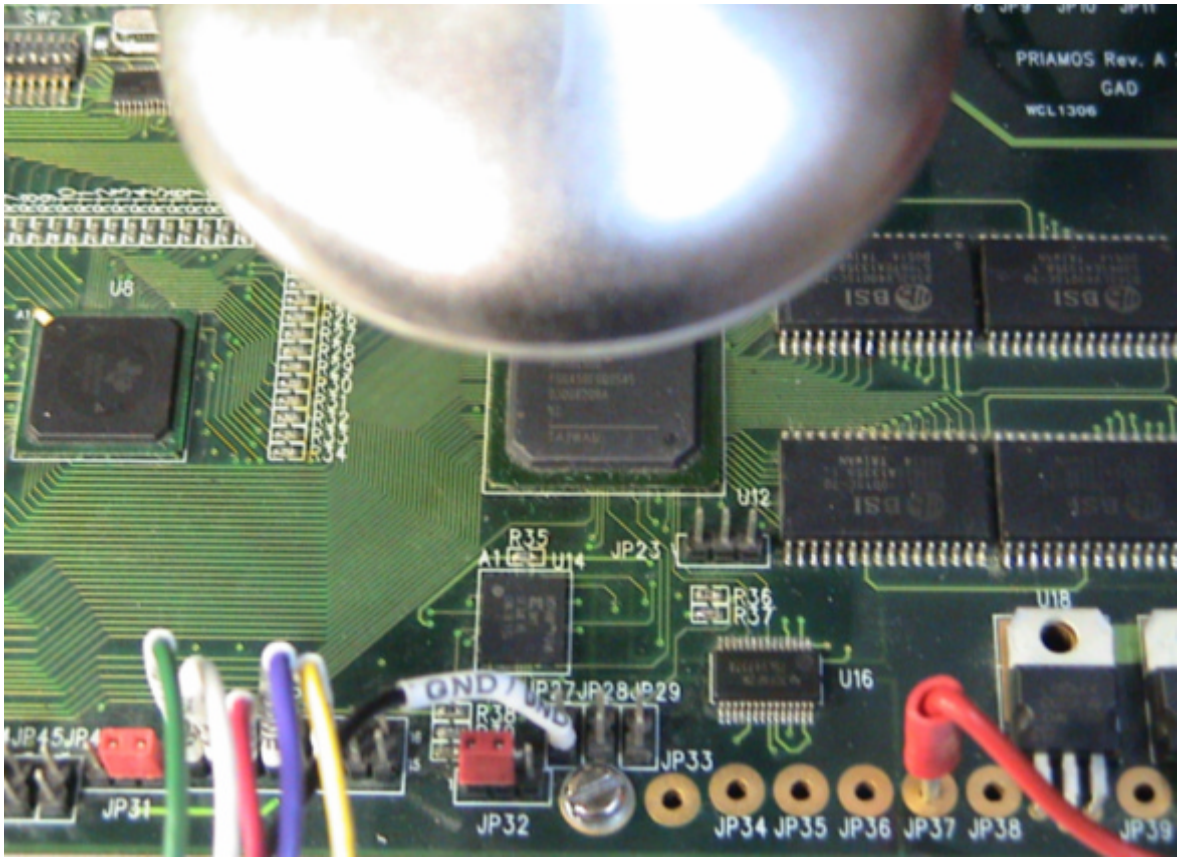

Figure D.12 DSP Engine Early Prototype Testing.

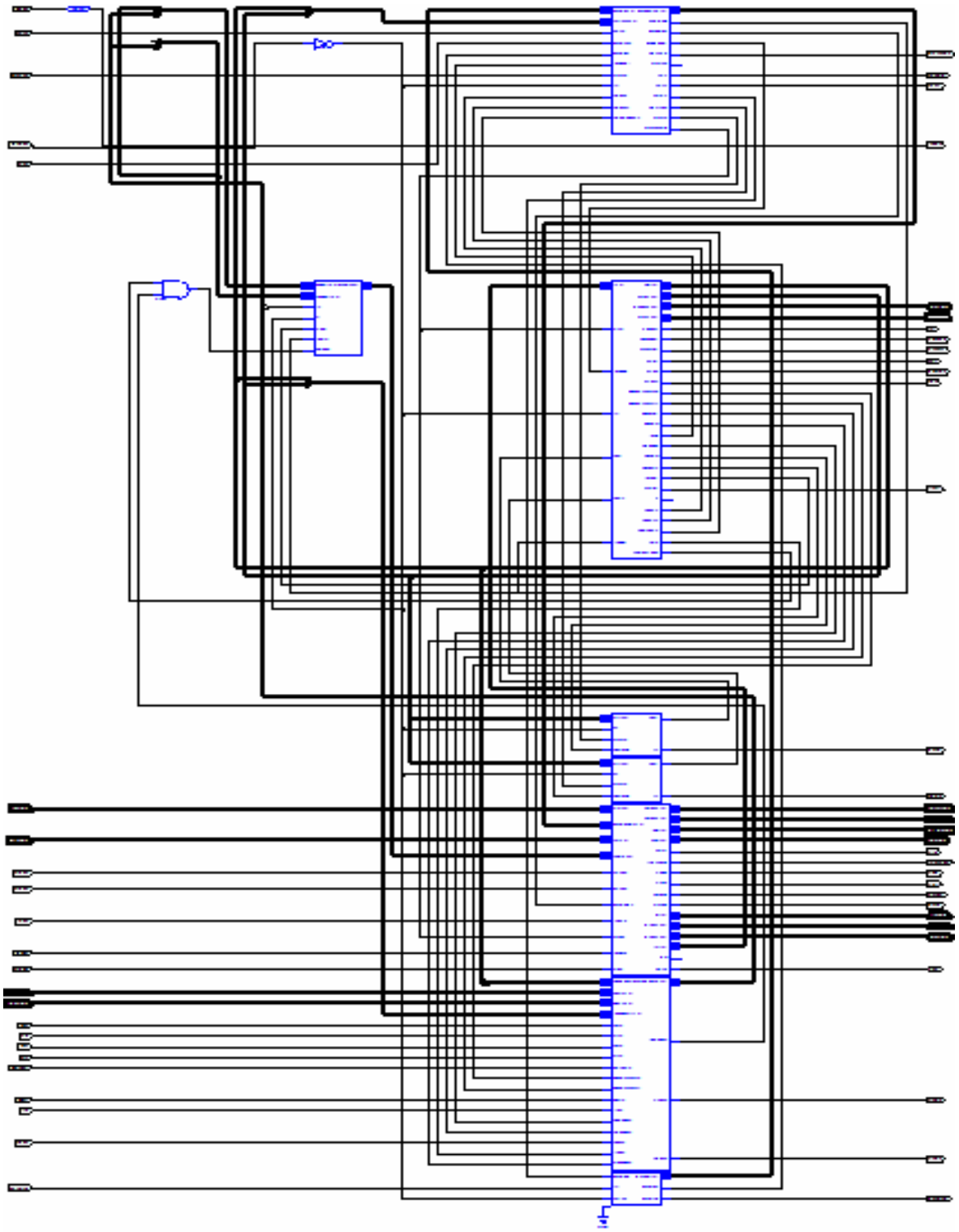

Figure D.13 Priamos DSP Engine FPGA Computer Architecture.

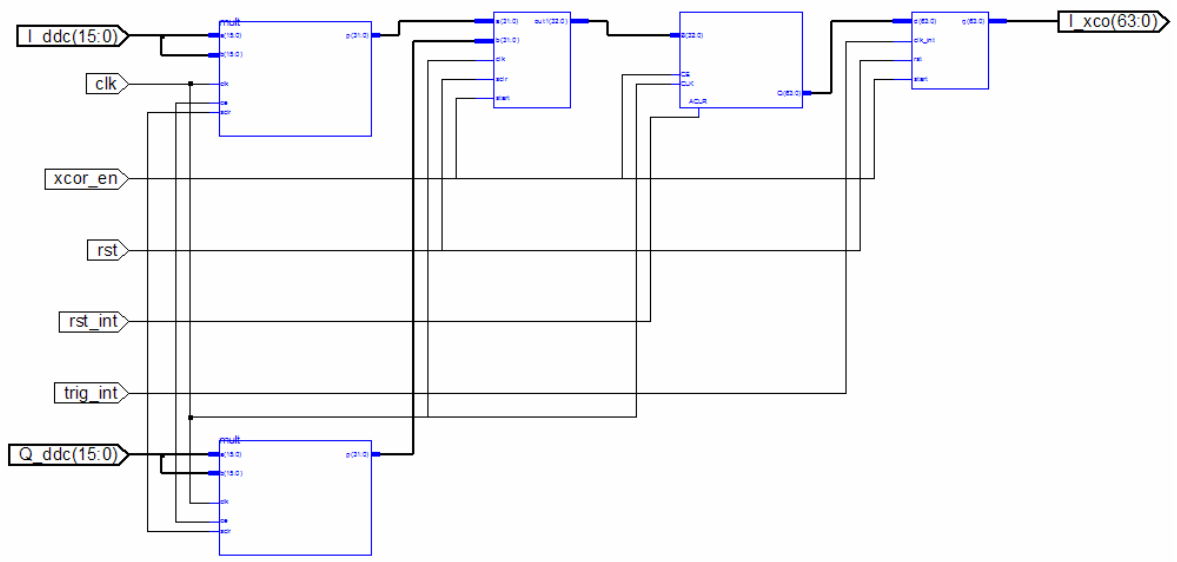

Figure D.14 Auto-Correlator Computer Architecture.

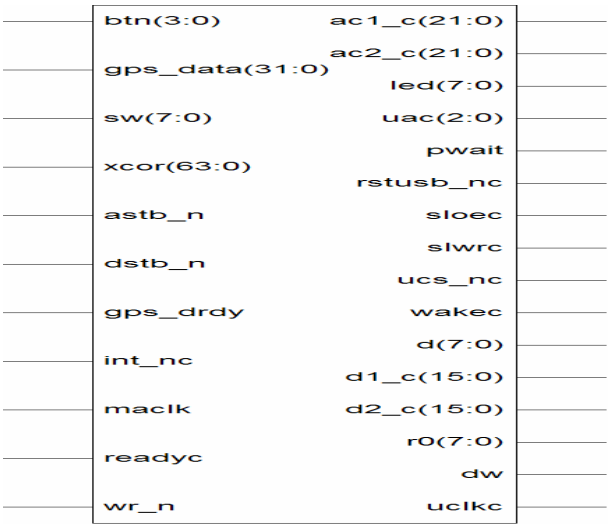

Figure D.15 Block Diagram for the Computer Engineering Interfaces.

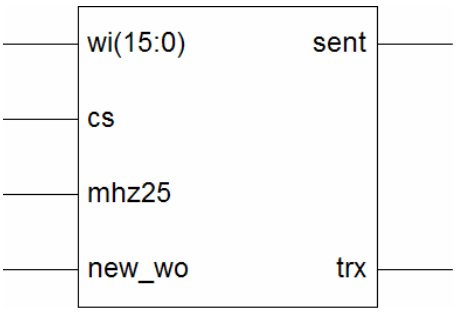

Figure D.16 Block Diagram for the Digital Amplifier Interface.

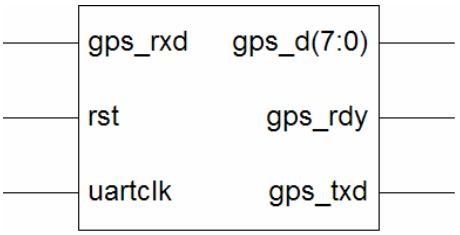

Figure D.17 Block Diagram for the GPS Interface.

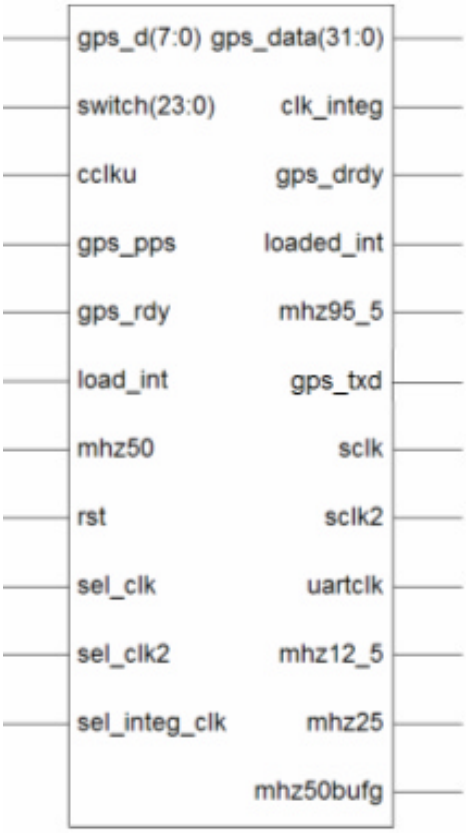

Figure D.18 Block Diagram for the Frequency Controller.

```
Design Summary
--------------
Number of errors:      0
Number of warnings:   19
Logic Utilization:
  Total Number Slice Registers:    12,798 out of  26,624   48%
    Number used as Flip Flops:                   12,766
    Number used as Latches:                          32
  Number of 4 input LUTs:          10,756 out of  26,624   40%
Logic Distribution:
  Number of occupied Slices:       10,786 out of  13,312   81%
Number of Slices containing only related logic: 10,786 out of 10,786 100%
    Number of Slices containing unrelated logic:   0 out of  10,786    0%
      Total Number 4 input LUTs:              11,872 out of  26,624   45%
  Number used as logic:                       10,756
  Number used as a route-thru:                   458
  Number used for Dual Port RAMs:                256
    (Two LUTs used per Dual Port RAM)
  Number used as Shift registers:                402
  Number of bonded IOBs:               214 out of     333   64%
    IOB Flip Flops:                     63
  Number of MULT18X18s:                  4 out of      32   12%
  Number of GCLKs:                       8 out of       8  100%

Total equivalent gate count for design:  280,835
Additional JTAG gate count for IOBs:      15,952
Peak Memory Usage:  493 MB

Design statistics:
   Minimum period:  10.428ns   (Maximum frequency:  95.896MHz)
   Minimum input required time before clock:  19.681ns
   Maximum output delay after clock:  27.178ns
```

Figure D.19 Priamos DSP Engine Design Summary.

Figure D.20 Priamos DSP Engine Unit.

Appendix E Dimagoras Hardware Design

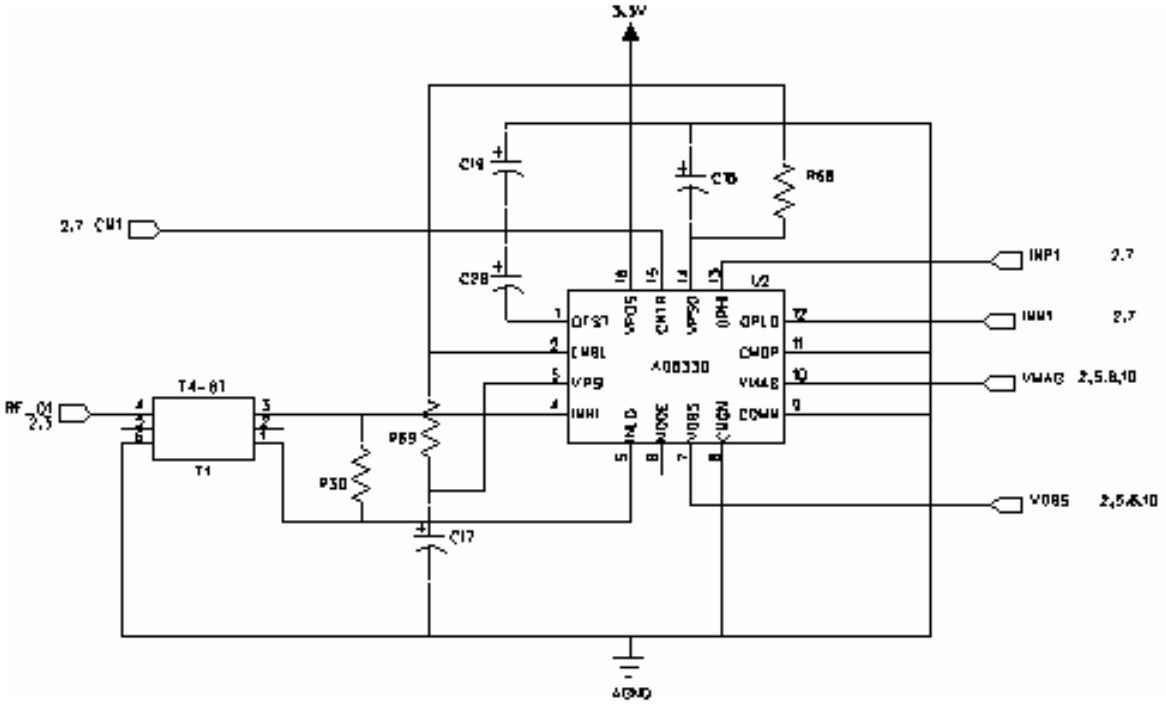

Figure E.1 Automatic Gain Controller Schematic.

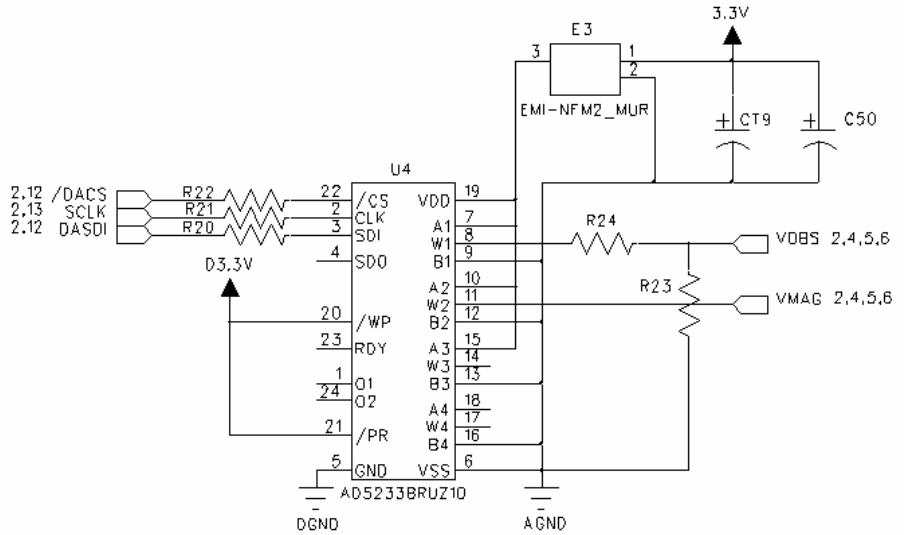

Figure E.2 Digital Potentiometer Schematic.

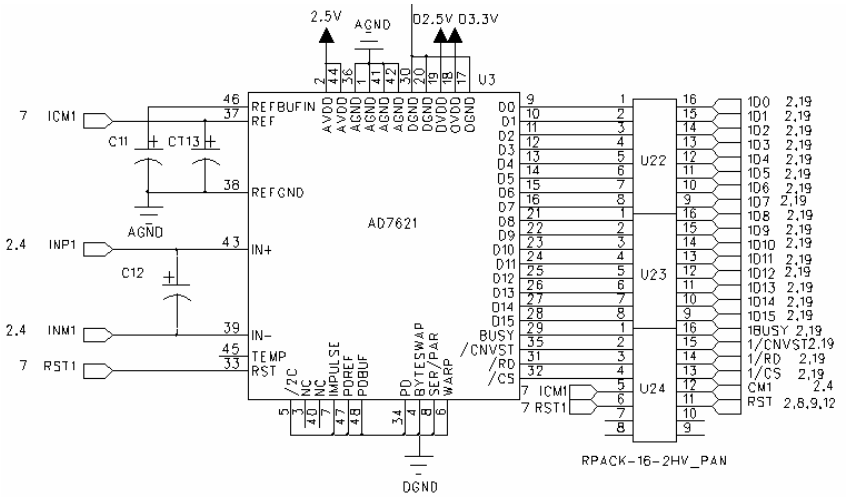

Figure E.3 ADC Schematic.

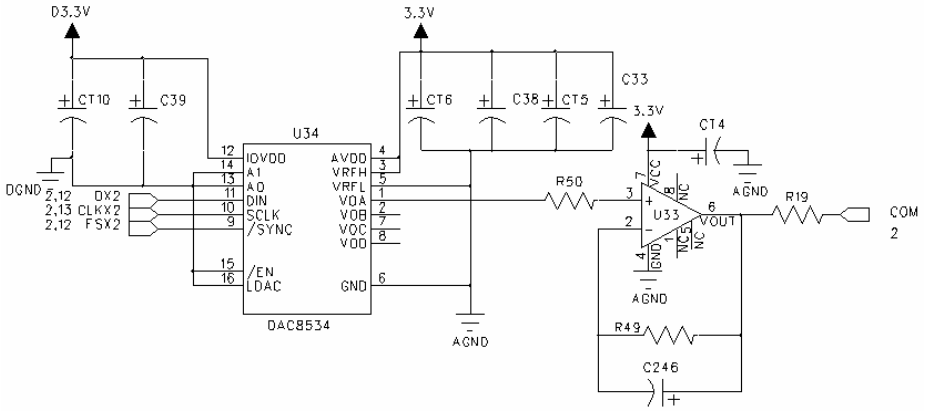

Figure E.4 DAC Schematic.

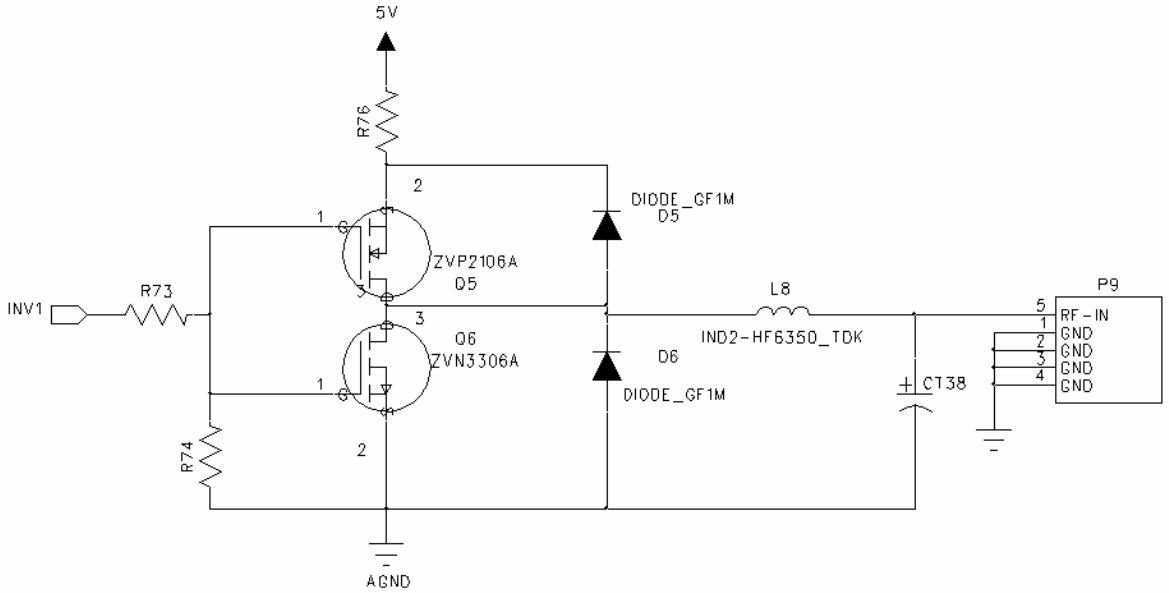

Figure E.5 Power Inverter Schematic.

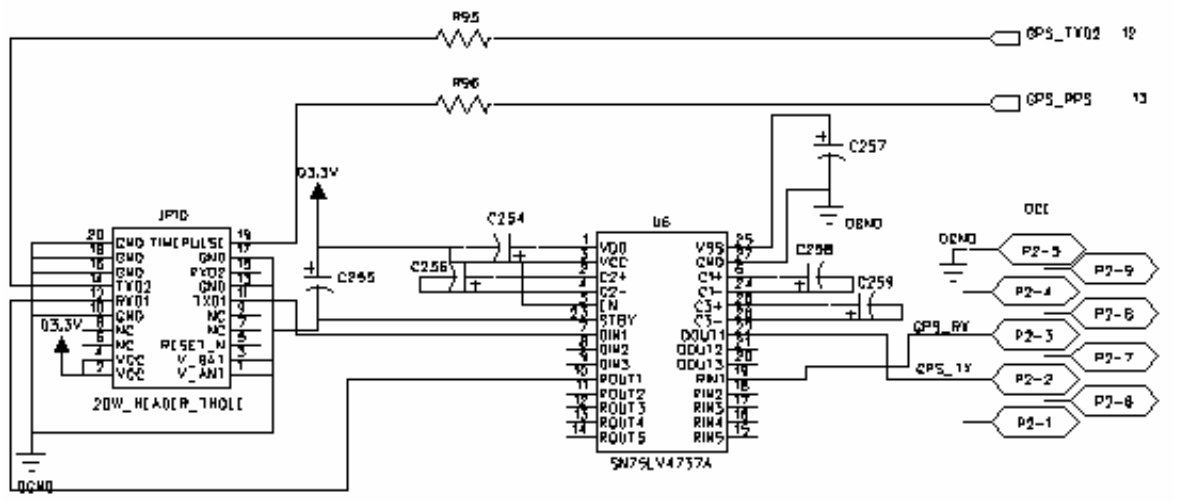

Figure E.6 GPS to FPGA, UART Interface Schematic.

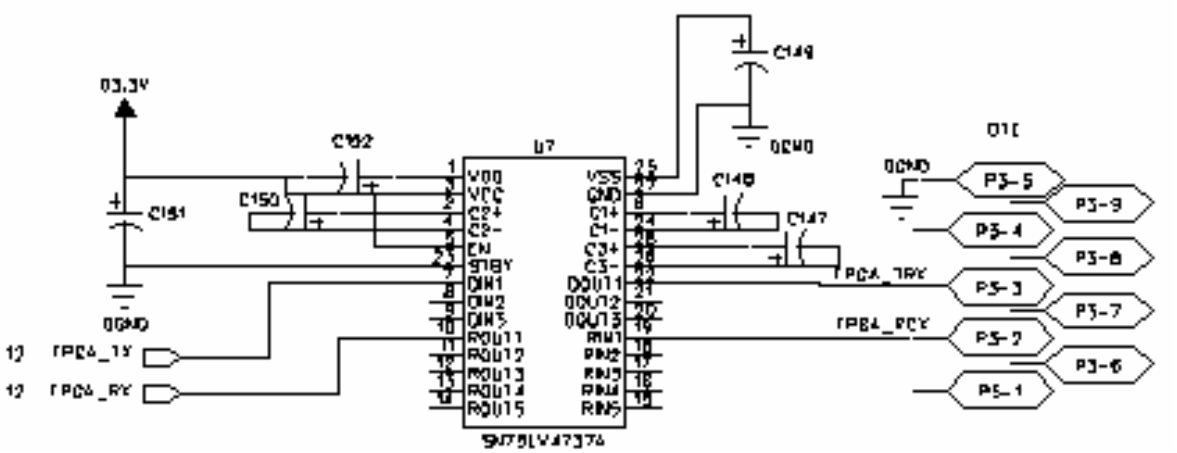

Figure E.7 FPGA to Host, UART Interface Schematic.

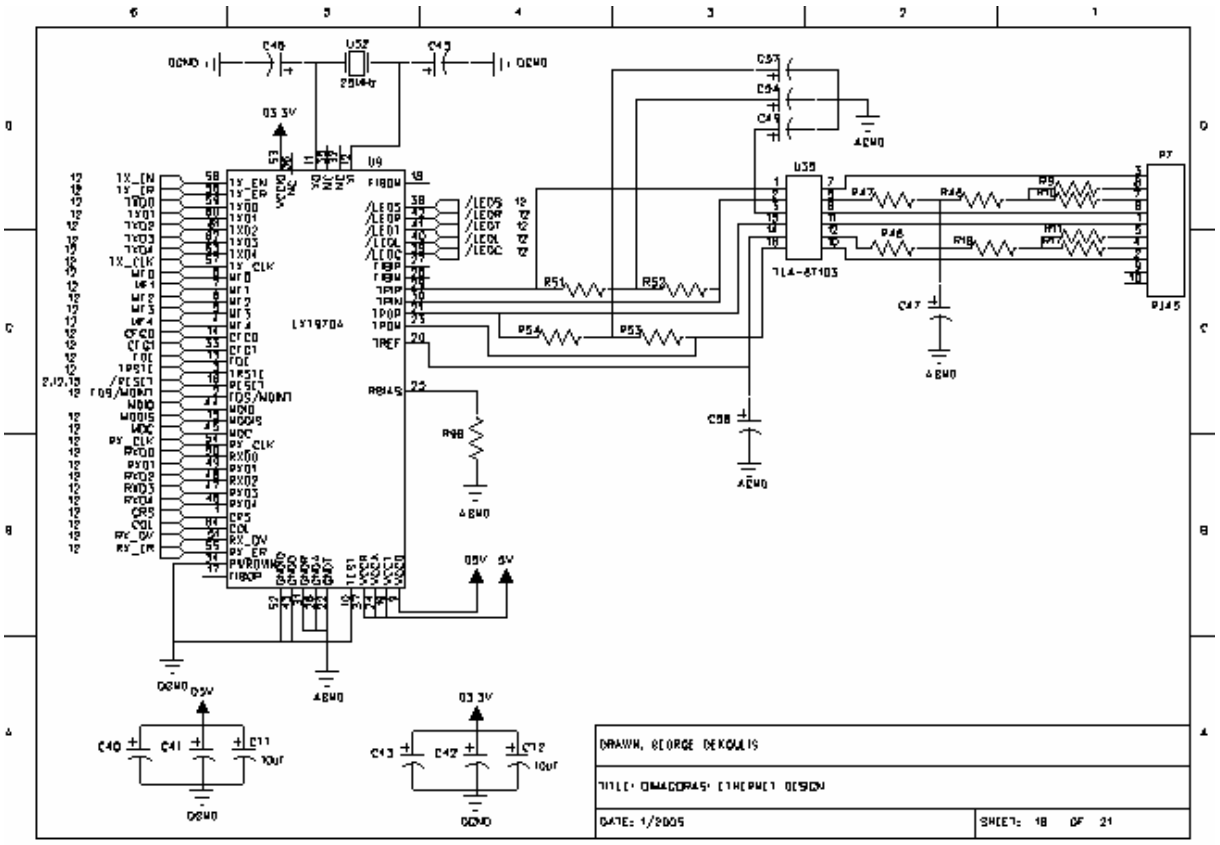

Figure E.8 10/100 Mbps Fast Ethernet Interface Schematic.

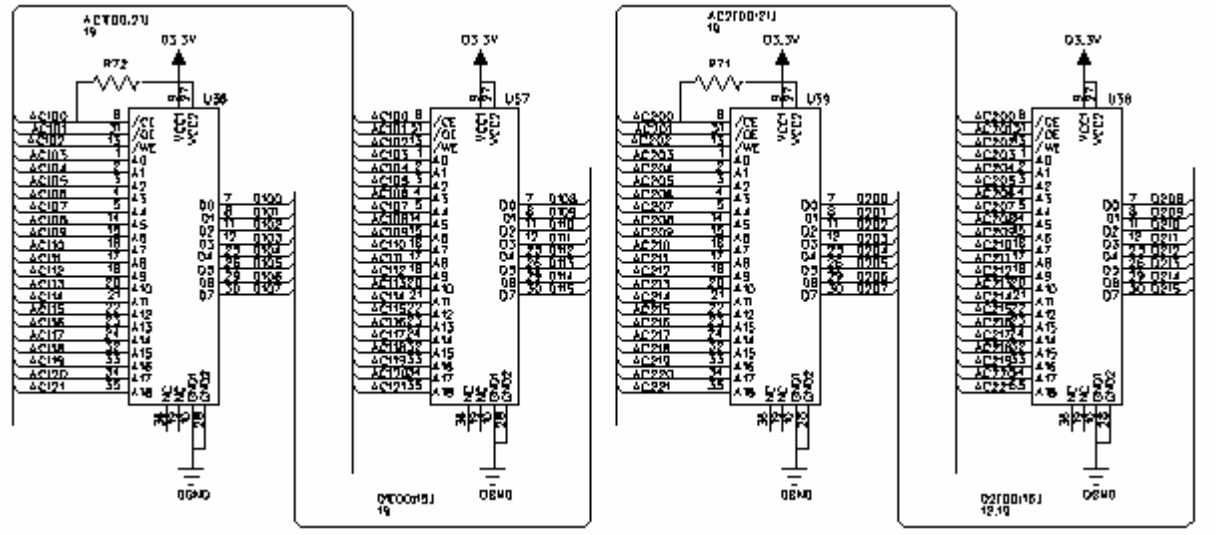

Figure E.9 16 Mbits SRAM Schematic.

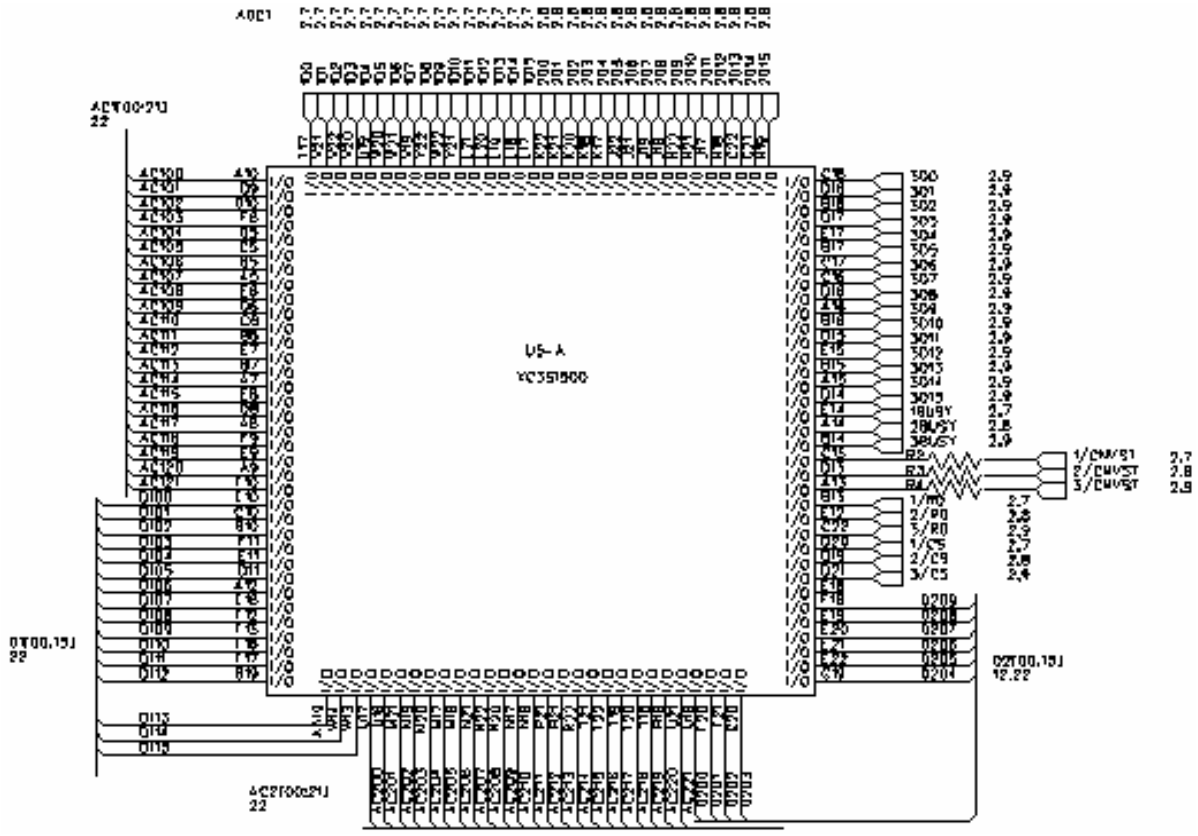

Figure E.10 FPGA I/O Interface 1.

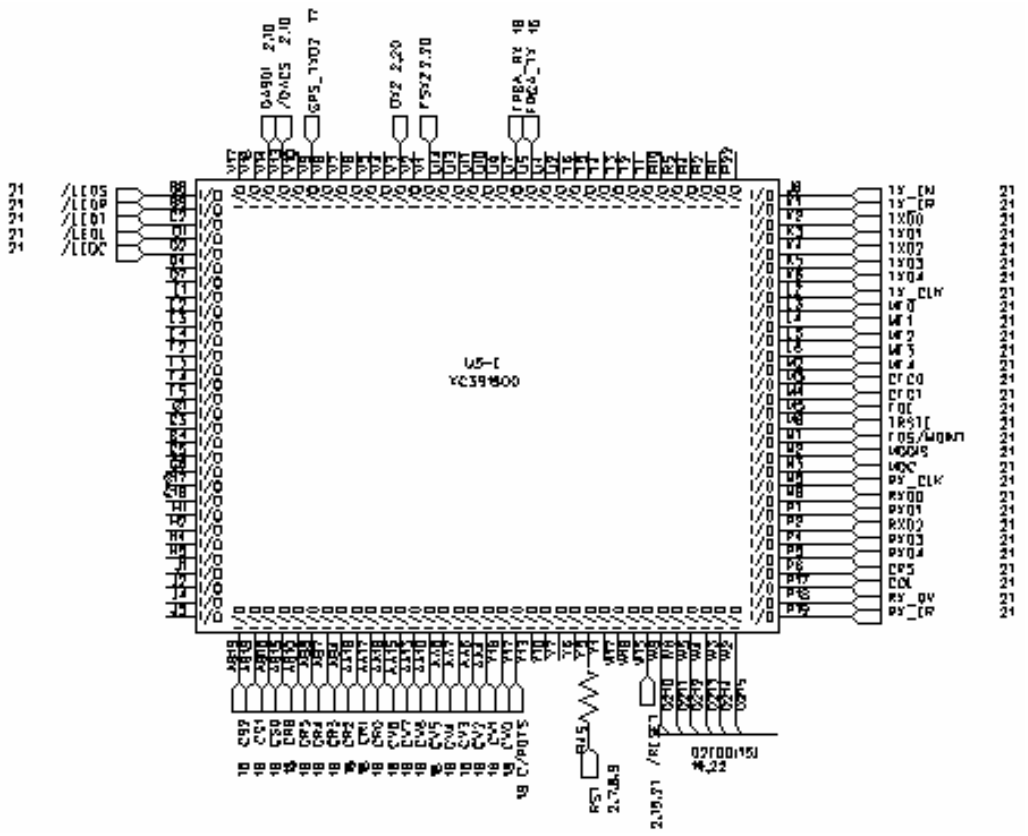

Figure E.11 FPGA I/O Interface 2.

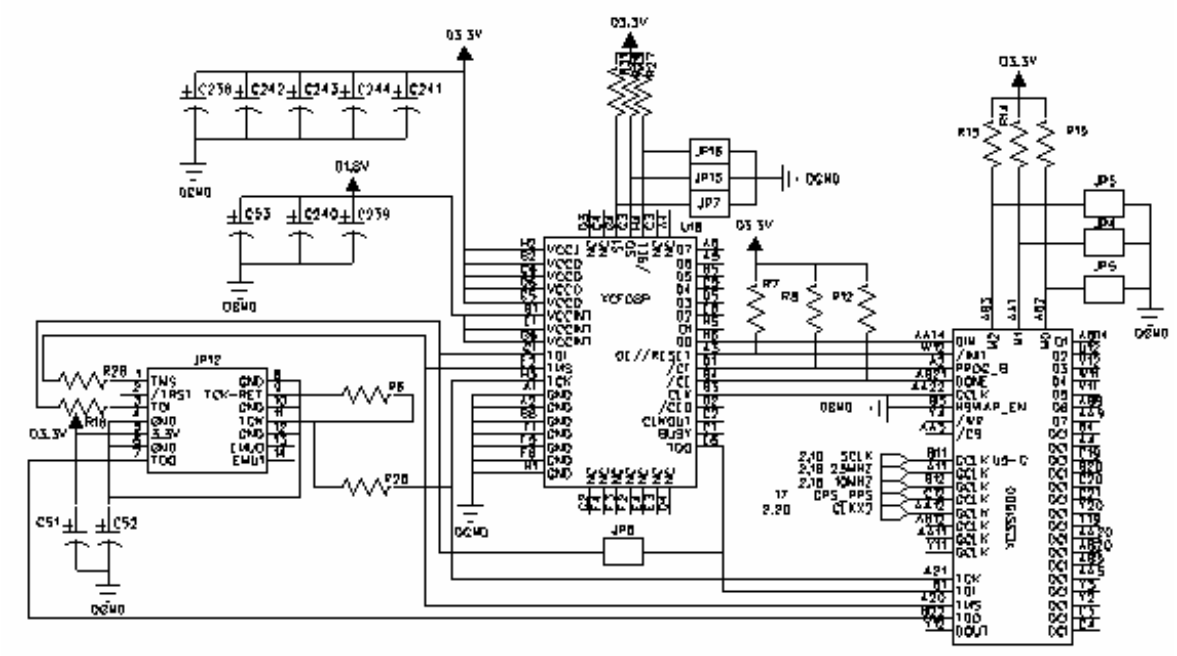

Figure E.12 FPGA Programming Interface.

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